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Thermal modeling of wire-bonded power modules considering non-uniform temperature and electric current interactions

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ABSTRACT

To assess power devices' reliability, it is crucial to have a relatively accurate thermal approach which provides valid temperature estimates. In this paper, a commercial Si IGBT and SiC MOSFET power modules are investigated. Also, the electric current-induced effects on bond wires and the correlation between the non-uniform temperature distribution and electrical conductivity of the sensitive constituent materials are studied. A more realistic active area of the die is defined by excluding inactive regions, i.e., the gate area, gate runners, and termination ring. Also, the electric current distribution among parallel bond wires attached to the dies' metalization pads is investigated. A comparison between an approach which includes all the above aspects with a conventional one where a thermal power with the same total value, but unifrom, is injected into the semiconductor dies is made, While an acceptable error is found for Si IGBTs, a very significant difference is observed in SiC MOSFETs.

1. Introduction

In the operation of power electronics converters, semiconductor devices are often the most vulnerable component. For example, in [1] it is presented that a significant proportion, almost 25%, of power converters' failures may arise in the semiconductor devices. Accordingly, the lifespan reliability of semiconductor devices becomes of great importance in early stages of development of power converters.

Among failure causes, the operating life of semiconductor devices is strongly influenced by the thermal cycling coming from a mission profile. For example, in [2] it is demonstrated that the temperature causes over 50% of failures where bond wire lift-off and solder joint fatigue are two primary thermal failure mechanisms due to the temperature swing (ΔT) and the difference in coefficients of thermal expansions (CTEs) of the constituent materials [3]. Consequently, an accurate knowledge of the semiconductor devices' temperature is indispensable to improve the converter reliability. The advantage of that can be better understood if one considers that a 10 °C change in a power device's temperature can result in approximately 50% change in the estimated lifespan [4].

Various approaches have been introduced in the literature to find power devices' surface temperature so far. One way is to integrate an NTC resistor or an on-die thermal diode into a device [5,6], but it needs fundamental design modifications and auxiliary external pins, which increase the manufacturing cost and introduce new reliability concerns.

Another way which has been introduced in some research works is the use of temperature-sensitive electrical parameters (TSEPs), e.g., the on-state voltage at low (sense) current levels [7]. However, the accuracy of TSEP approaches is an intrinsic limit together with the measurement circuit complexity. Furthermore, TSEPs provide an average temperature of the die rather than the surface temperature distribution [8].

One may use optical methods such as optical fibers [9], and infrared cameras [10] in order to map the devices' temperature. Nevertheless, they require an intrusive modification of the device (e.g., removal of the package or dielectric insulating gel) such that they are not applicable for on-line measurement during the converter operation.

Many research works have focused on the use of numerical methods such as finite element method (FEM) [11], finite difference method (FDM) [12], and finite volume method (FVM) [13], in order to mimic as accurate as a possible experimental condition. The difference between these methods is the mathematical models or governing equations used for the computation. FEM is used by most simulators as it allows a relatively fair approximation with lower calculations when compared with two other ones [14].

Although numerical methods give an accurate temperature distribution of devices, limitations have been found, which are rarely addressed in the literature so far. One of the limitations is that the

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power loss/heat is typically assumed to be independent of electrical variables, hence uniformly dissipated in the die, whereas, given the significant temperature dependence of semiconductor characteristics and the fact that the die's temperature distribution is always non-uniform [15], the assumption of uniform power dissipation can hardly be established.

Moreover, the presence of bond wires is often neglected in thermal models. In [16], though, a higher current density is shown to occur at the interfaces between bond wires and the die with respect to other regions on the die's active area which can also influence the temperature distribution.

In the literature, the whole volume of the die is often defined as an active area in which the electric power is turned into heat. It is well known, though, that the active area's size is smaller than the whole die one because the dies are typically surrounded by a termination ring and encompass a gate area and often gate runners passing through them. This reduced volume changes the resulting electric current density and in turn, can affect the temperature distribution of the die as well.

In this paper, two commercial Si IGBT and SiC MOSFET power modules have been selected to be studied through FEM simulations in order to obtain accurate and detailed temperature distributions. In this way, different thermal models are analyzed and compared in order to investigate effects of temperature-dependent electrical conductivity, electric current-induced bond wires, and more realistic active area's geometry.

2. Power modules under study

In this study, a commercial Si IGBT (IFS75B12N3E4) and a commercial SiC MOSFET (CCS050M12CM2) power module are studied, which have the same voltage/current ratings of 1200 V/75 A (see Fig. 1). The thermal stack of both modules comprises direct bonded copper (DBC) substrate, Sn3.0Ag0.5Cu (SAC305) solder joints, and copper baseplate. Detailed specifications of the layers have been provided in Table 1. The temperature dependency of the thermal properties, i.e., thermal conductivity and specific heat capacity, have been taken into account for Si, SiC, and Al_2O_3 materials, according to [17,18], as they can affect the temperature estimation by several degree Celsius [19]. In addition, a forced cooling system as a convective heat transfer coefficient, *htc*, which is applied to the baseplate's backside has been considered in the study.

Table 1
Detailed specifications of constituent layers of the selected power modules.

Layer material	Thickness (μm)	Density (kg/m^3)	Thermal conductivity (W/m·K)		Specific heat capacity (J/kg·K)	
			Temp. (°C)	Value	Temp. (°C)	Value
Si die	120	2329	25	148.0	25	705.0
			125	98.9	125	788.3
			225	76.2	225	830.7
SiC die	180	3240	25	353.3	25	551.8
			125	257.7	125	585.1
			225	202.8	225	634.0
DBC Al_2O_3	380	3965	25	37.0	25	785.5
			125	27.2	125	942.0
			225	20.9	225	1076.0
Die solder	100	7370	All	57.0	All	220.0
DBC copper	300	8960	All	401.0	All	385.0
Baseplate solder	250	7370	All	57.0	All	220.0
Baseplate	3000	8960	All	401.0	All	385.0

3. Proposed modeling approach

3.1. Die physical modeling

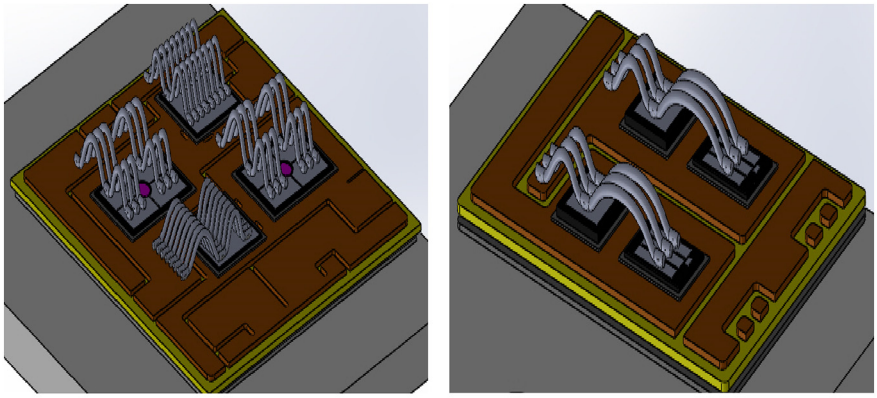
In semiconductor dies, the gate pad is located either in the center or the corner of the die, which is electrically isolated from the emitter or source metallization. Gate runners which cross the die's topside metallization pads are used to provide a low-impedance path to distribute the gate signals with a minimum propagation delay. Furthermore, a termination ring surrounding the die provides the necessary high-voltage isolation (see Fig. 2). The above regions do not contribute to the die's active area. Therefore, the active area is smaller than the whole die's one and, in addition, consists of separated sections.

3.2. Temperature-dependent electrical conductivity

When operating the power module, power losses generated by conduction and switching processes are turned into heat. By defining the locations of *a* and *b* at the center and corner of a specific die, respectively, one can find the following relationship:

$$T_a - T_b = \Delta T = \alpha P \tag{1}$$

where T is the temperature, P is power loss, and $\alpha = \frac{d\delta}{\lambda A}$ is a constant coefficent. λ is thermal conductivity, A and $d\delta$ are cross-sectional area



(a) (b)

Fig. 1. 3D model of the selected power modules' layout: (a) Si IGBT, (b) SiC MOSFET.

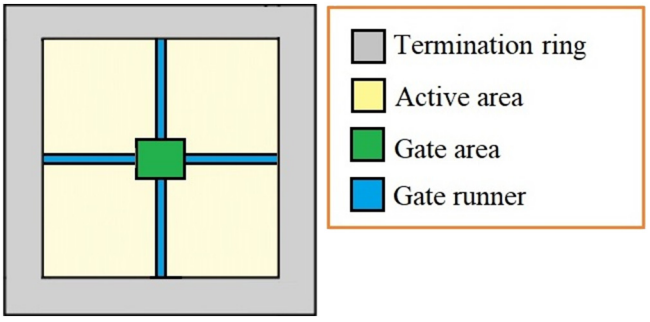


Fig. 2. Typical die's layout.

of the path, and the distance between the observed positions *a* and *b*, respectively.

It is worth to note that, in most of the cases, the temperature of different points of the die would not be equally increased. For example, Fig. 3a shows a snapshot of an IGBT die temperature recording acquired by an IR camera. As shown in the picture, the maximum temperature occurs in the center, whereas the minimum occurs in the corner of the die. Fig. 3b displays the time waveforms at points Sp1 and Sp2 of Fig. 3a. In [20] it is mentioned that the non-uniformity of temperature distribution becomes more severe at higher power losses.

On the other hand, electrical characteristics provided in power devices' datasheet by manufactures exhibit a noteworthy temperature dependency. A typical I–V curve of semiconductor dies has been shown in Fig. 4. If we apply such I–V curve to the elementary cells of the dies, then one can conclude that for a given on-state voltage, the current through each cell would depend on its temperature. In other words, during real operation and being the same voltage on the die's metallization pads, there would be a non-uniform, temperature-dependent current distribution within the die's volume.

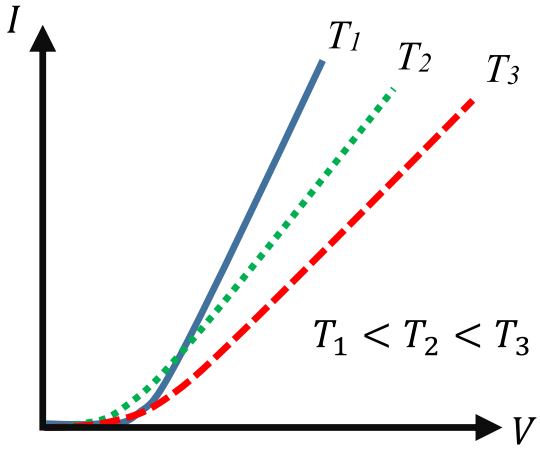
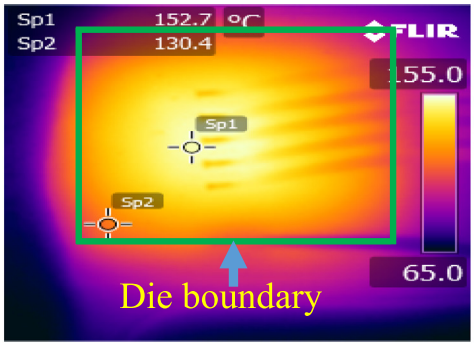


Fig. 4. Typical temperature-dependent I–V characteristics of semiconductor dies.

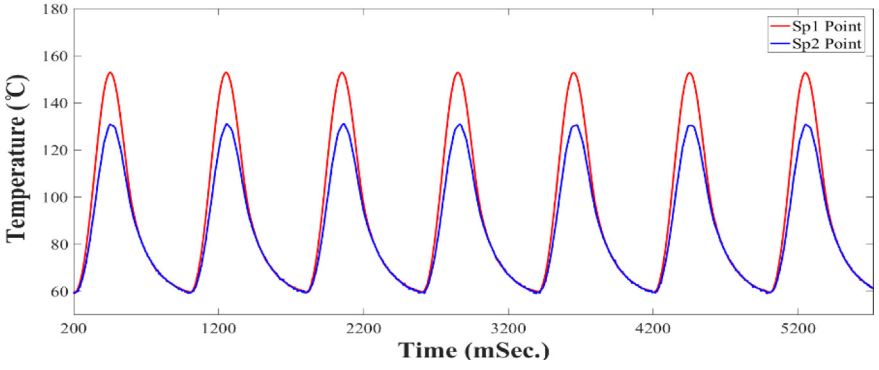
An efficient way to take the above effect into account is to introduce an equivalent electrical conductivity. The electrical conductivity of a semiconductor die can be in general calculated by a simple mathematical equation as follows:

$$\sigma = \frac{d}{R \bullet A} \tag{2}$$

where d is the thickness, A is a cross-sectional area, and R is the electrical resistance of the die. In Fig. 5, the equivalent electrical conductivity calculated by Eq. (2) for the selected Si IGBT and SiC MOSFET dies from the available datasheets has been shown. As Fig. 5 shows, the variation of the electrical conductivity of SiC die is higher than that of Si one.



(a)



(b)

Fig. 3. (a) Temperature map of Si IGBT die, (b) temperature cycles of points 'Sp1' and 'Sp2' defined in (a).

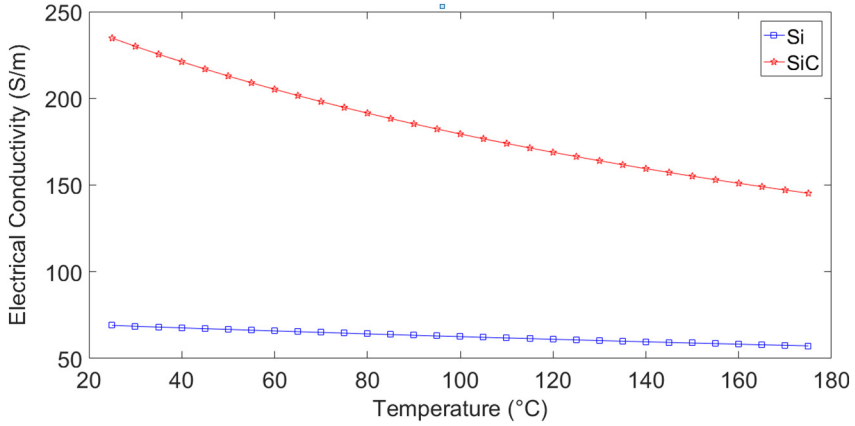


Fig. 5. Electrical conductivity of the Si IGBT and SiC MOSFET dies of the selected power modules.

In addition, the temperature-dependent resistivity of the pure aluminum and copper metals can be implemented by a linear approximation as below [21]:

$$\rho(T) = \rho_0[1 + \beta(T - T_0)] \tag{3}$$

where β is a temperature coefficient, T_0 is a fixed reference temperature, and ρ_0 is the resistivity at T_0. In [21], one can find $\rho_0 = 2.65 \times 10^{-8}\ \Omega\cdot$m and $\alpha = 0.00404\ \mathrm{K}^{-1}$ for the pure aluminum, and $\rho_0 = 1.68 \times 10^{-8}\ \Omega\cdot$m and $\alpha = 0.00390\ \mathrm{K}^{-1}$ for the pure copper, all at $T_0 = 20^{\circ}$C.

4. Simulation results

In this paper, six study cases are investigated for both Si IGBT and SiC MOSFET power modules as described in the following, so that the thermal models become more and more complete from Case I to Case VI. Boundary conditions have been set to the ambient temperature $T_a = 25\,^{\circ}$C and $htc = 1500\ \mathrm{W/m^2{\cdot}K}$ representing a forced water cooling system [22]. It is also worth noting that temperature-dependent thermal properties of sensitive materials are intended for all of the case studies.

Case I. Thermal model with uniform heat generation, and the whole die as the active area.

This approach has been widely used in the literature referred to as conventional one where bond wires and dies' metallization pads are ignored. In addition, power losses are modeled as uniform heat sources spread over the die volume.

Case II. Thermal model with uniform heat generation and more realistic active area.

The purpose of choosing this case is to investigate the effect of the considering a more realistic active area on the dies' temperature distribution in comparison to the previous case. It means that inactive regions, i.e., the gate area, gate runners, and termination ring are removed.

Case III. Thermal model with uniform applied voltage and more realistic active area.

In this case, an electric potential, i.e., the on-state voltage, is uniformly applied to the dies' top surface instead of injecting uniform heat. Constant equivalent electrical conductivities have been employed here. The equivalent electrical conductivities of both Si and SiC dies are set to the ones at 100 °C.

Case IV. Thermal model with uniform applied voltage, temperature-dependent electrical conductivity, and more realistic active area.

Looking for a complete model, the motivation of this study case is to investigate the effect of the temperature-dependent electrical conductivity of the dies (see Fig. 5) on the temperature distribution.

Case V. Thermal model with bond wires, uniformly applied voltage, and more realistic active area.

In this study case, the model introduced as Case III is completed by adding wires bonded to dies' topside metallization pads. Then, similar electric potential values are applied to bond wires. The purpose is to study the effect of electric current-induced bond wires on the temperature distribution.

Case VI. Thermal model with bond wires, uniformly applied voltage, temperature-dependent electrical conductivity, and more realistic active area.

This approach is a more complete one of Case V which includes temperature-dependent equivalent electrical conductivity of dies, or it is a more complete of Case IV which includes electric current-induced bond wires. This study case implements the most complete structure among the six study cases.

Note that the silica gel, which is generally potted into power modules has been ignored in this paper because it has no significant effect on the temperatures of devices. Fig. 6 shows a precise step-by-step procedure to build a structure closer to the reality, i.e., Case VI, which should be taken for more accurate reliability assessments.

The results of the study cases obtained through FEM implemented in COMSOL Multiphysics environment have been presented in Table 2. They show that the active area, input type (i.e., heat or voltage), the bond wires, and temperature-dependent electrical conductivities would affect the dies' temperatures. Also, it is found that the variation of temperatures due to upgrading the conventional model (Case I) to the complete model (Case VI) are larger for SiC MOSFET in comparison to Si IGBT due to a higher variation of the electrical conductivity of SiC die with temperature in contrast to Si one.

The results obtained for Si IGBT die establish that the change of active area from the whole die to a more realistic volume decreases the maximum temperature by nearly 2%. Furthermore, the inclusion of constant or temperature-dependent electrical conductivities decreases the maximum temperature by nearly 5%, and the addition of bond wires together with constant or temperature-dependent electrical conductivities increases the maximum temperature by nearly 11%. These results for SiC MOSFET die are nearly +4%, +6%, +20%, −19%, +18%, respectively. However, if the conventional approach, Case I, is upgraded to the most complete approach, Case VI, which includes all the above considerations, then the maximum temperature of Si IGBT and SiC MOSFET dies will be increased by 4% and 28%, respectively.

The thermal resistance for each constituent layer of the devices can be defined as:

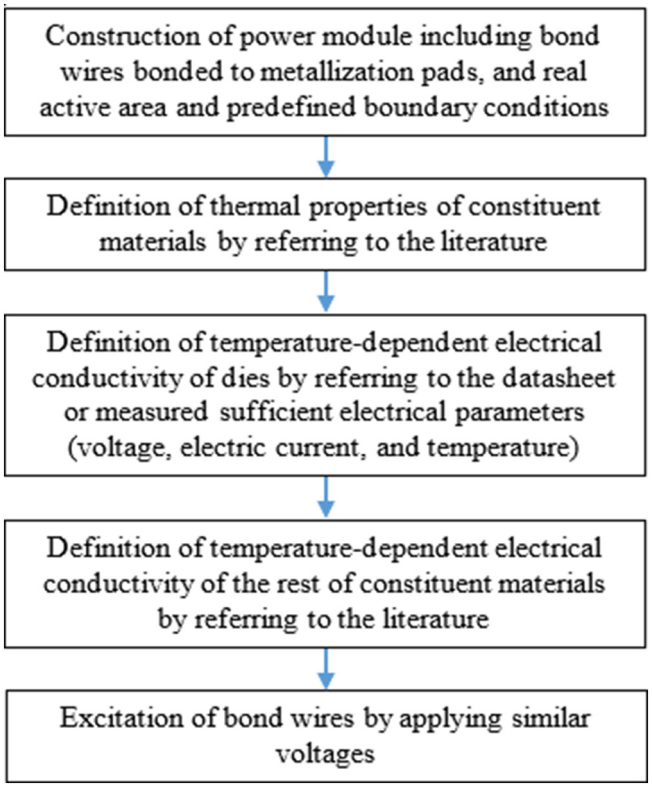


Fig. 6. A flowchart of the structure proposed to find more accurate temperature distribution.

$$R_{th} = \frac{d}{A \bullet \lambda} \tag{4}$$

where d is thickness, A is the cross-sectional area, and λ is the thermal conductivity of the related layer.

We know $\lambda_{MOSFET} > \lambda_{IGBT}$, but in this study we have $d_{MOSFET} > d_{IGBT}$ and $A_{MOSFET} < A_{IGBT}$ from the physical structures of the devices. For example, at a specific temperature of 125 °C, we have $\lambda_{MOSFET} = 257.7$ W/(m·K), and $\lambda_{IGBT} = 98.9$ W/(m·K). Also, $d_{MOSFET} = 180$ µm, $d_{IGBT} = 120$ µm, $A_{MOSFET} = 26.02$ mm^2, and $A_{IGBT} = 70.32$ mm^2. By these values and using Eq. (4), one can obtain $R_{th,\,j} = 0.0268$ W/K and 0.0173 W/K for the die (semiconductor layer) of SiC MOSFET and Si IGBT, respectively (the subscript j stands for the junction). Therefore, one can conclude for the studied devices, while the SiC material is thermally more conductive than Si material, the SiC die has a larger $R_{th,\,j}$ than Si die because of the geometry. In addition, the area of thermal path is affected by that of the die in other words, a smaller SiC area results in a narrower thermal path within the underlying layers. It means that while the thickness and material of the thermal stack for both SiC MOSFET and Si IGBT are similar, according to Eq. (4) there is a larger $R_{th,\,ts}$ for the SiC MOSFET's thermal stack in comparison to Si IGBT's one (the subscript ts stands for the thermal stack). Therefore, at the same power loss, the SiC MOSFET's junction will reach higher temperature with regards to the following equation.

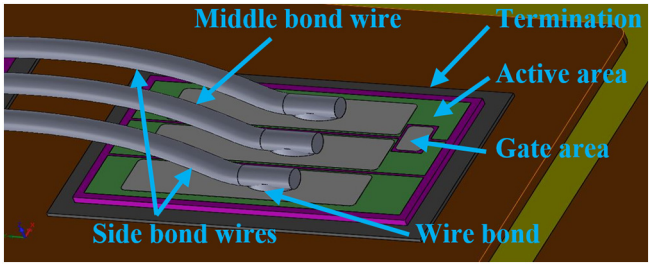


Fig. 7. Internal structure of the studied SiC power module around the MOSFET die.

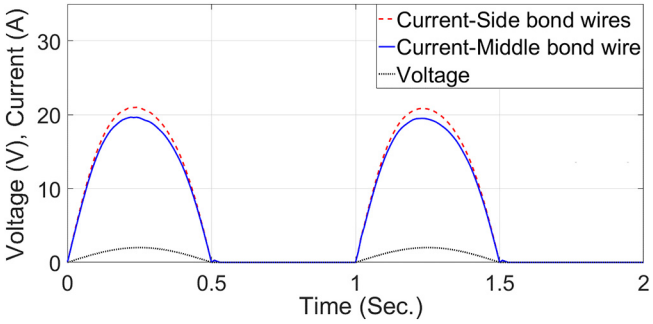


Fig. 8. Current distribution among the parallel bond wires of the SiC MOSFET die. The driving signal is a periodic half-wave voltage, and the approach is Case VI.

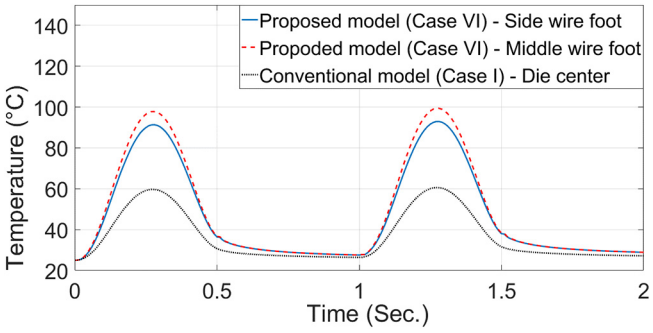


Fig. 9. The temperature profile of the center point of the wire feet of the SiC MOSFET die for Case VI and Case I (conventional approach).

Table 2
Temperature range (°C), on-state voltage (V), and electric current (A) of Si IGBT and SiC MOSFET dies due to applying the same total power loss/heat of 100 W for different study cases (Note: Case VI has been defined as a reference).

Module Type	Parameter	Case I (conventional)	Case II		Case III		Case IV		Case V		Case VI	
		Value	Value	Change (%)	Value	Change (%)	Value	Change (%)	Value	Change (%)	Value	Change (%)
Si IGBT	Max. temp.	90.4	88.6	−2.0	84.4	−6.6	84.4	−6.6	94.6	4.6	94.0	4.0
	Min. temp.	71.5	71.4	−0.1	68.3	−4.5	68.5	−4.2	69.7	−2.5	69.4	−2.9
	Voltage	–	–	–	1.8	–	1.7	–	2.12	–	2.03	–
	Current	–	–	–	56.3	–	58.3	–	47.1	–	49.1	–
SiC MOSFET	Max. temp.	129.7	134.4	3.6	142.5	9.9	168.1	29.6	143.2	10.4	166.0	28.0
	Min. temp.	102.6	98.2	−4.3	107.9	5.2	127.2	24.0	91.9	−10.4	105.4	2.7
	Voltage	–	–	–	1.88	–	1.8	–	2.09	–	1.93	–
	Current	–	–	–	53.2	–	56.3	–	47.9	–	51.8	–

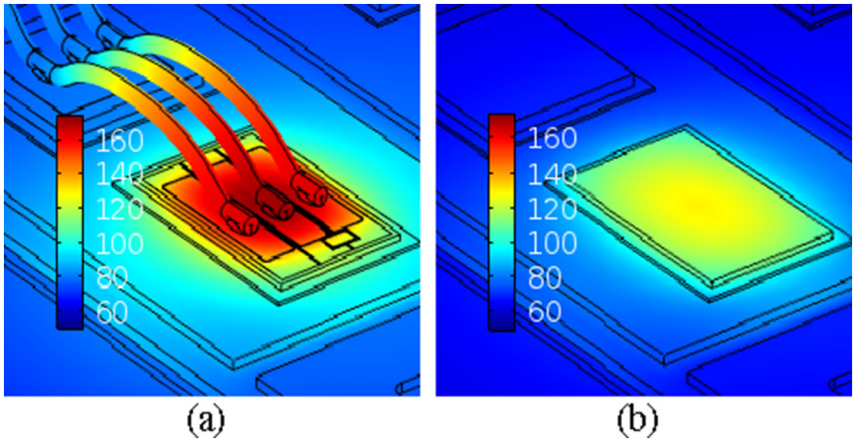


Fig. 10. Temperature distribution of SiC MOSFET die at the steady state for the same dissipated power loss/heat: (a) The most complete structure (Case VI) with $V = 1.93\,\text{V}$ and $I_{tot} = 51.8\,\text{A}$, (b) conventional approach (Case I) with the uniformly dissipated power $P = 1.93\,\text{V} \times 51.8\,\text{A} = 100\,\text{W}$.

$$T_j = P_{loss} \bullet R_{th,jb} \tag{5}$$

where T_j is the junction temperature, P_{loss} is the power loss, and $R_{th,jb}$ is the equivalent thermal resistance between the junction and baseplate.

For the sake of completeness, the electro-thermal behavior of SiC MOSFET is described in the following because it is more influenced by the previous considerations in respect to Si IGBT. Fig. 7 shows the layout of SiC MOSFET die on which three bond wires are placed. The electric current distribution generated by a half-wave on-state voltage (equal to that in Case VI of Table 2) waveform at the frequency of 1 Hz has been shown in Fig. 8. One can find from Fig. 8 that the electric current flowing into the middle wire is lower than that of side wires. This is due to higher temperatures, as shown in Fig. 9, and consequently less electrical conductivity at the die's central area on which the middle wire is bonded.

In Fig. 9, one can find much higher transient temperatures for the Case VI in comparison to the conventional approach, Case I. In Fig. 10, temperature distributions of both approaches above have been shown at the steady state for a similar power loss of 100 W. Again, one can observe higher temperatures for Case VI in comparison to the conventional approach.

5. Conclusion

This paper shows the thermal difference between Si IGBT and SiC MOSFET power modules studied through FEM including electric current-induced bond wires, a more realistic active area of dies, and temperature-dependent thermal and electrical properties of materials. The results show that by considering the aspects above, a small error in the estimated temperature of the Si IGBT die is obtained if compared to the conventional approach referred to Case I in this paper. However, in the case of the SiC MOSFET power module, the error is very significant. For example, the error in the maximum temperature estimated for the most complete structure, i.e., Case VI with reference to Case I has been found to be 4% and 28% for the studied Si IGBT and SiC MOSFET power modules, respectively. Thus, a more accurate structure, especially for SiC devices, is highly recommendable to be employed. This is crucial for engineers that need to perform accurate simulations to better predict the junction temperature of the device for online condition monitoring and reliability assessment, where the temperature distribution is a decisive factor.

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