# Non-uniform Temperature Distribution Implications on Thermal Analysis Accuracy of Si IGBTs and SiC MOSFETs

Mohsen Akbari*[1], Amir Sajjad Bahman[2], Paula Diaz Reigosa[2], Lorenzo Ceccarelli[2], Francesco Iannuzzo[2], Mohammad Tavakoli Bina[1]

[1] Power Electronics Laboratory, K. N. Toosi University of Technology, Tehran, Iran
[2] Center of Reliable Power Electronics (CORPE), Aalborg University, Aalborg, Denmark

* Corresponding Author: mohsen.akbari.eng@gmail.com

*Abstract*

*Being the power loss and temperature distribution in power-electronics semiconductor dies influenced by one another, this paper demonstrates that neglecting such an effect can result in significant errors in electro-thermal simulations and mistaken calculation of junction temperatures. Two case studies on different semiconductor technologies, namely Silicon Insulated-Gate Bipolar Transistors (IGBTs) and Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), are presented to corroborate the paper findings. Resultant temperature distributions are obtained by a proposed flowchart, which accepts the corresponding power dissipation input from MATLAB environment and employs a finite element based analysis implemented in COMSOL Multiphysics environment.*

## 1 Introduction

The knowledge of die temperatures of power semiconductor devices, which is interpreted to junction temperatures, is of great importance in order to ensure the reliable design of converters and safe operation. Thermal images captured by infrared (IR) cameras show that the temperature of the converter's components, e.g., semiconductor dies might have a large non-uniform distribution [1-2].

The non-uniform temperature distribution within the die is not a new topic, and it has been investigated in few research works so far. In [3], the non-uniform temperature of IGBT dies is introduced as thermal stress to degrade the device performance and system reliability significantly; in the same paper, a thermoelectric solid-state cooling system embedded in a direct bonded copper (DBC) substrate is proposed to make IGBT chip temperature more uniform. Also, it is shown that an increase in effective heat transfer coefficient (*htc*) will reduce the IGBT temperature but will not affect the temperature distribution on the IGBT surface. Furthermore, it can be seen that the maximum temperature variation – the difference between the maximum and minimum temperatures on the IGBT surface – increases with the IGBT power loss approximately by almost twice. In [4], the lateral gradient (spatial derivative) of silicon (Si) IGBT die temperature is utilized to detect the location and degree of voids and/or delamination at the solder joints. In [5], a temperature spectrum density method (TSDM) is proposed based on statistic characteristics of thermal images for the condition monitoring of IGBT modules.

As mentioned before, the non-uniform temperature distribution of devices can be used for the condition monitoring of the devices. In addition, such a non-uniform distribution might make unbalanced thermal stresses on bond wires and underlying layers, especially die solder joint. Thereby, the temperature distribution is itself a constructive or exacerbating factor for failures, e.g., bond wire lift-off, and cracks/voids in the die solder joint. Therefore, a knowledge of temperature distribution of devices can be of great importance in the reliability study.

To find the temperature distribution, one can employ some experimental techniques. In [2], the influence of the lateral gradients on the measurement of the junction temperature by means of the widely used $V_{CE}(T)$-method has been investigated. It is found that temperatures obtained from measurements correspond to the current-weighted average. However, such a technique need a complicated measurement circuit and might reduce the device efficiency. Another way is the use of an IR camera to map the device temperature [1-2]. Although this method presents accurate temperature distributions, it needs the device to be decapsulated, which is not applicable during the device operation.

Considering limitations in experimental techniques and thanks to nowadays' powerful computational tools, thermal simulations of devices can be developed to evaluate the device reliability. Numerical methods, e.g., finite element method (FEM) [6], finite volume method (FVM) [7], finite difference method (FDM) [8], and Fourier series [9] are introduced to thermally model and analyze the devices with significant accuracy. It is worth noting to mention that in this paper, COMSOL Multiphysics software, which employs FEM, has been selected to simulate devices under study in order to find temperature distributions of the devices.

In addition, it should also be pointed out that in thermal models presented in the past research works, a simplification is made and it is that temperature distribution - power dissipation interactions are never investigated.

Based on the datasheet, one can find a high-temperature dependency on the electric currents flowing through the

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devices. In Fig. 1, typical static electric current-voltage (I-V) curves of semiconductor devices are shown at different temperatures [11]. It can be seen that in the positive temperature coefficient (PTC) region, the higher the temperature of the semiconductor die, the lesser the electric current density, hence power loss. This case is opposite in the negative temperature coefficient (NTC) region, i.e., low electric currents. The interaction will be more severe in the future when the power density of dies increases to more than 1,000 W/cm$^2$ – today it is in the range of 100-500 W/cm$^2$ – due to the trend towards device miniaturization and high performance [12-14]. High power density can make temperature differences between the center and the corners of a chip exceed even 50K. Therefore, for such a high-temperature difference, the role played by the temperature distribution becomes very critical in respect to reliability issues.

In this paper, in order to examine the temperature- loss interaction, Silicon Insulated-Gate Bipolar Transistors (Si-IGBTs) and Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC-MOSFETs) devices are selected. A three-dimensional (3-D) model of the devices is designed in FEM simulations to calculate the temperature distribution. This analysis is combined with MATLAB to obtain a correct non-uniform power distribution within dies by referring to electrical curves available in the datasheet.

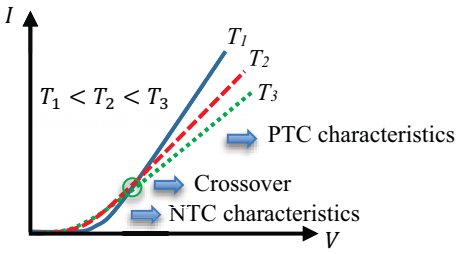


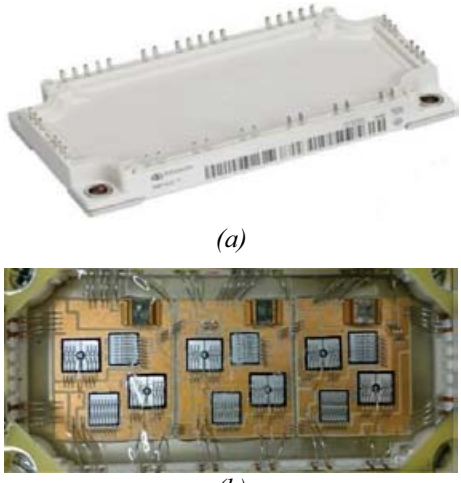

*Figure 1: Typical static temperature-dependent I-V characteristics of power semiconductor devices (dies)*

## 2 Case studies

In this work, two types of power modules, namely Si IGBT and SiC MOSFET, with similar current and voltage ratings of 75 A / 1200 V have been selected. The IGBT module is the IFS75B12N3E4 [15] manufactured by Infineon Technologies with a die size of 7.71×9.12×0.12 mm$^3$, which is shown in Fig. 2. The selected SiC MOSFET is the CCS050M12CM2 [16] manufactured by Cree Inc. having a die size of 6.44×4.04×0.18 mm$^3$, which is shown in Fig. 3. Figs. 2 and 3 illustrate the packaged and opened devices.

It is worth noting that both power modules have the same thermal stack including SnAgCu (SAC) solder joints, Direct Bonded Copper (DBC) substrate, and copper baseplate.

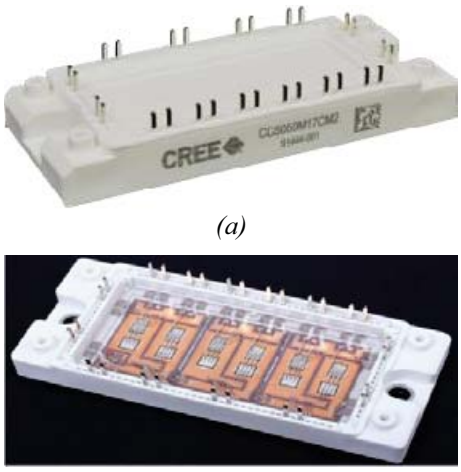
The effect of the cooling system is handled by applying a convective *htc*, to the backside of the baseplate. The use of the parameter *htc* instead of a real cooling system simplifies the study system and reduce the time of computation. In this study, the value of 100,000 W/(m$^2$·K) is considered for the parameter *htc*, which represents a heatsink equipped with the condensing water vapor [17]. Such a high *htc* parameter almost makes a constant temperature equal to the ambient temperature at the backside of the baseplate. Also, the ambient temperature is defined as 25℃., the temperature dependency of thermal conductivities is taken into account because they might cause temperature errors to a few degrees [18]. Table 1 lists the characteristics of the constituent layers for each module as well as the temperature-dependent thermal conductivities for the thermo-sensitive layers. Note that to find the thermal conductivities at other temperatures, a linear interpolation is utilized.



*(a)*

*(b)*

*Figure 2: (a) packaged (b) opened Si IGBT module*




*(a)*

*(b)*

*Figure 3: (a) packaged (b) opened SiC MOSFET module*

## 3 Methodology

The flowchart of the proposed technique is provided in Fig. 4. For the sake of a fair comparison, the dissipated power $P_{ref}$ ("reference power") is forced to be the same in both cases. The proposed approach is iterative, and it is described as follows. First, the surface power density distribution $\rho_{Pref}(x,y)$, which is a uniform distribution, is calculated by

$$\rho_{P_{ref}} = \frac{P_{ref}}{A} \quad (1)$$

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*Table 1: Material layer characteristics of the power modules*

| Layer material | Thickness (µm) | Density (kg/m³) | Thermal conductivity (W/m·K) | | Specific heat capacity (J/kg·K) | |
|---|---|---|---|---|---|---|
| | | | Temp. (°C) | Value | Temp. (°C) | Value |
| Si die | 120 | 2329 | 25 | 148.0 | 25 | 705.0 |
| | | | 125 | 98.9 | 125 | 788.3 |
| | | | 225 | 76.2 | 225 | 830.7 |
| SiC die | 180 | 3240 | 25 | 353.3 | 25 | 551.8 |
| | | | 125 | 257.7 | 125 | 585.1 |
| | | | 225 | 202.8 | 225 | 634.0 |
| DBC Al2O3 | 380 | 3965 | 25 | 37.0 | 25 | 785.5 |
| | | | 125 | 27.2 | 125 | 942.0 |
| | | | 225 | 20.9 | 225 | 1076.0 |
| Die solder | 100 | 7370 | all | 57.0 | all | 220.0 |
| DBC copper | 300 | 8960 | all | 401.0 | all | 385.0 |
| Baseplate solder | 250 | 7370 | all | 57.0 | all | 220.0 |
| Baseplate | 3000 | 8960 | all | 401.0 | all | 385.0 |

where $A$ is top side area of the die «1» (the symbol « » shows the corresponding output in the related flowchart, which is shown in Fig. 4). Note that the top surface dissipation is usually used, especially in normal operations. Because most of the heat is generated across the channel region, which is located on the die surface in the range of either few microns for modern trench technology or few nanometres for old planar technology. After applying the power density distribution to the top side of the die, the initial temperature distribution $T_1(x,y)$ ($k$=1) is worked out «2». Then the temperature distribution is fed to the static power density-voltage ($\rho_P$-$V$) curves at a given on-state voltage $V_1$. The static curves have been extracted from the datasheets, which are implemented in MATLAB in the form of lookup tables. Accordingly, the updated power density distribution $\rho_{P(updated)}$ is worked out «3», and then it is spatially integrated in order to calculate the overall dissipated power, $P_k$ «4». The error of the resultant overall power in respect to the reference power is calculated by subtracting «5» and then the output is multiplied by a constant factor $C_f$ «6». The output is used to update the previous on-state voltage «7» via an accumulator. The $V_{k(updated)}$ and $T_k(x,y)$ are fed into the $\rho_P$-$V$ lookup table, to find the power density distribution of the next iteration $\rho_{P,k+1}(x,y)$ «8». Again, $\rho_{Pk+1}(x,y)$ is fed to the finite simulation to find the temperature distribution of the current iteration $T_{k+1}(x,y)$. The process continues until the calculated error «5» will be less than 0.1 W.

## 4 Simulation

The models of the IGBT and MOSFET power modules, as shown in Fig. 5, are built to study through the FEM. Note that in this work to reduce the simulation time, only one leg (left side) of the three-leg modules is investigated.

It is worth to mention that in the FEM simulation, a mesh optimization has been made to find an optimal number of finite elements so that at the same boundary conditions and inputs when the mesh is refined, electro-thermal results will no longer change; in other words, errors due to the mesh size will be negligible. In fact, meshing optimization yields a balance between the accuracy of the results and the simulation time. Thereby, the number of finite elements for the IGBT and MOSFET sections under study is found equal to 57,998 and 49,529, respectively.

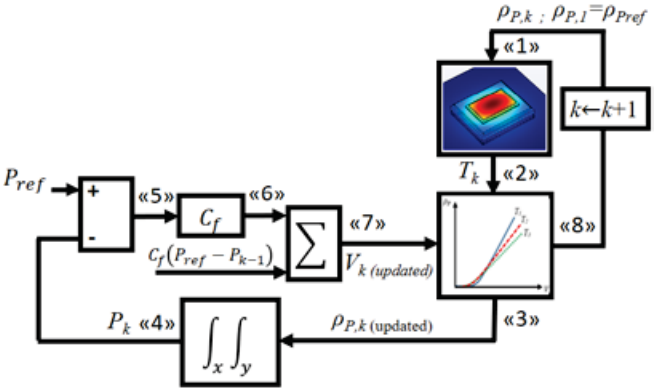


*Figure 4: Proposed flowchart to find the temperature-dependent power dissipation, which is fitted with the temperature distribution*

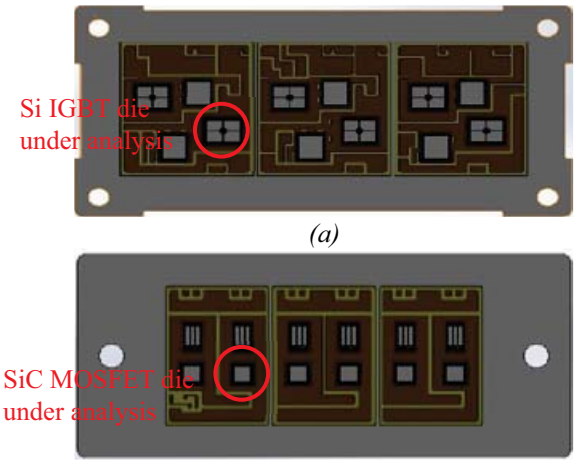


*Figure 5: Modules' models (a) Si IGBT (b) SiC MOSFET*

## 5 Results

In this section, simulation results are discussed for different power losses injected to the top surface of dies. When running the COMSOL-MATLAB co-simulations, solutions of the flowchart shown in Fig. 4 have converged to $P_{ref}$ in maximum 50 iterations. The obtained temperatures for the top surface of both Si IGBT and SiC MOSFET dies are provided in Figs. 6-8 at 100W, 200W, and 300W total power loss, respectively.

In Figs. 6-8, the effect of both uniform and temperature-dependent power losses is investigated. A more detailed temperature results are also listed in Table 2. One can find from these results that the non-uniformity of the power dissipation obtained for SiC MOSFET introduces higher error than that for the case of Si IGBT and in turn, SiC MOSFET temperatures are more influenced by the non-uniform power dissipation.

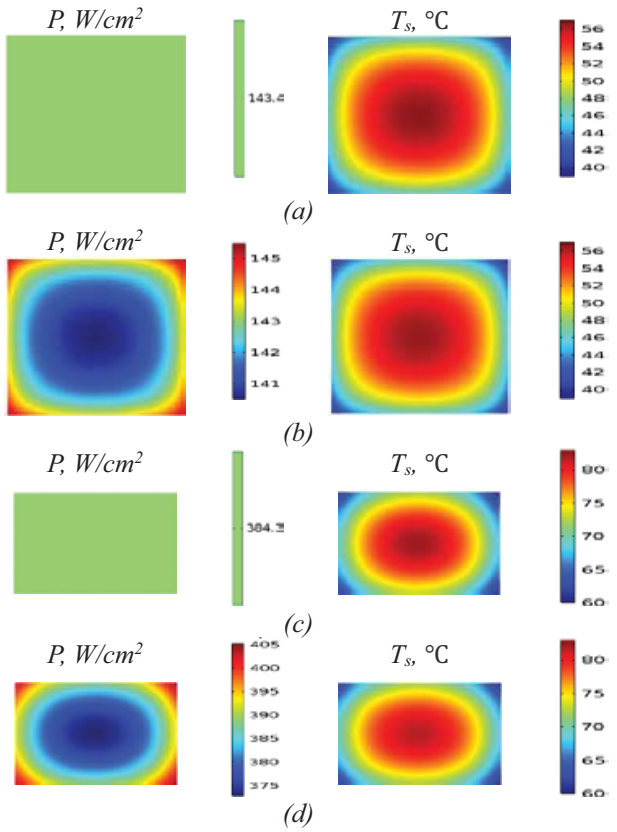


*Figure 6: Top surface distribution of steady-state power density, $\rho_P(x,y)$, and temperature, $T_s(x, y)$, for a total heat of 100 W, htc = 100,000W/(m²·K), and $T_a$=25 °C: (a) Si IGBT uniform heat dissipation, (b) Si IGBT non-uniform heat dissipation, (c) SiC MOSFET uniform heat dissipation, (d) SiC MOSFET non-uniform heat dissipation*

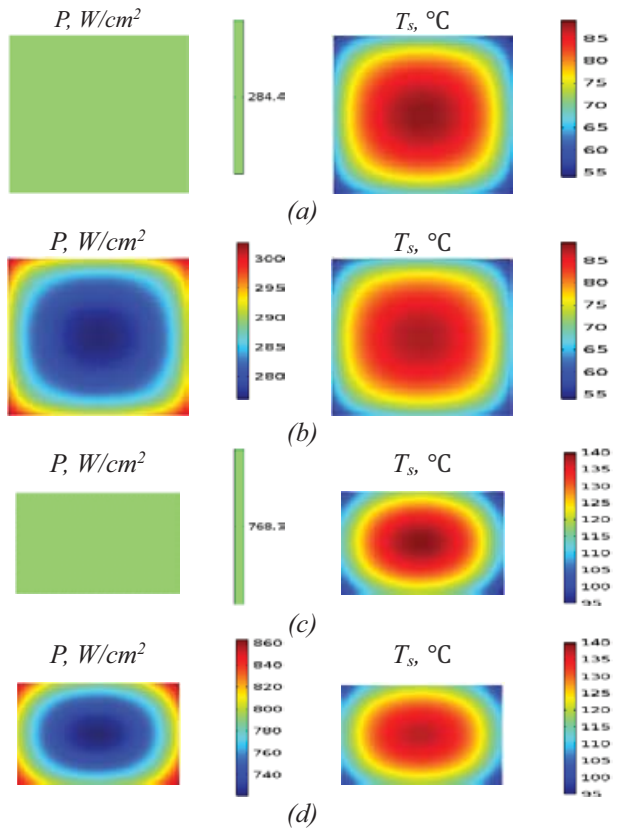


*Figure 7: Top surface distribution of steady-state power density, $\rho_P(x,y)$, and temperature, $T_s(x, y)$, for a total heat of 200 W, htc = 100,000 W/(m²·K), and $T_a$ = 25 °C: (a) Si IGBT uniform heat dissipation, (b) Si IGBT non-uniform heat dissipation, (c) SiC MOSFET uniform heat dissipation, (d) SiC MOSFET non-uniform heat dissipation*

The reason is due to the SiC material properties which leads to a much higher variation of electric current/electrical resistance/power loss with the temperature (~100% variation in the range of 25 °C-175 °C for the case study) in comparison to those of the Si IGBT (~20% variation in the range of 25 °C-175 °C for the case study). The non-uniform heat dissipation results in decreasing the maximum temperatures and increasing the minimum temperatures. Thereby, the temperature difference ($\Delta T_s$) between the center and corner of the dies decreases in comparison to a case where a uniform heat dissipation is considered. In addition, when increasing the total power, the difference between the obtained temperatures from uniform and non-uniform power dissipations increases. In other words, with increasing the total power loss, its non-uniform distribution effect on the die's temperatures becomes more critical. Therefore, one can conclude that neglecting the interaction between temperature and power loss at high power losses can result in very significant errors, especially in the case of SiC devices. Note that the advantage of SiC devices is that they can withstand high-temperature operation (150 °C-200 °C), while Si devices should operate at low temperature, usually lower than 150 °C [19].

## 6 Implications on reliability estimation

An application of the results found in this work can be used for the lifetime estimation of semiconductor devices. One can find several methods to evaluate the end-of-life of semiconductor devices in [20-21]. For example, the number of cycles to failure, $N_f$, can be obtained from the Coffin-Manson-Arrhenius model expressed as [20]:

$$N_f = \mathrm{C} \times \left(\Delta T_{j,t}\right)^{-\alpha} \times exp\left(\frac{E_a}{k_B \times T_{jm,t}}\right) \quad (2)$$

where $\Delta T_{j,t}$ is junction (active area) temperature fluctuation ($T_{jmax,t}$ - $T_{jmin,t}$) at a specific location in the die, $T_{jm,t}$ is mean temporal temperature ($T_{jmax,t}$ + $T_{jmin,t}$)/2, $C$ and α are the lifetime model parameters, which are assumed to be 97.2 and 3.1, respectively derived from accelerated aging experiment's results [22]. $E_a$ is activation energy ($9.89\times10^{-20}$ J), and $k_B$ is Boltzmann constant ($1.38\times10^{-23}$ J·K$^{-1}$).

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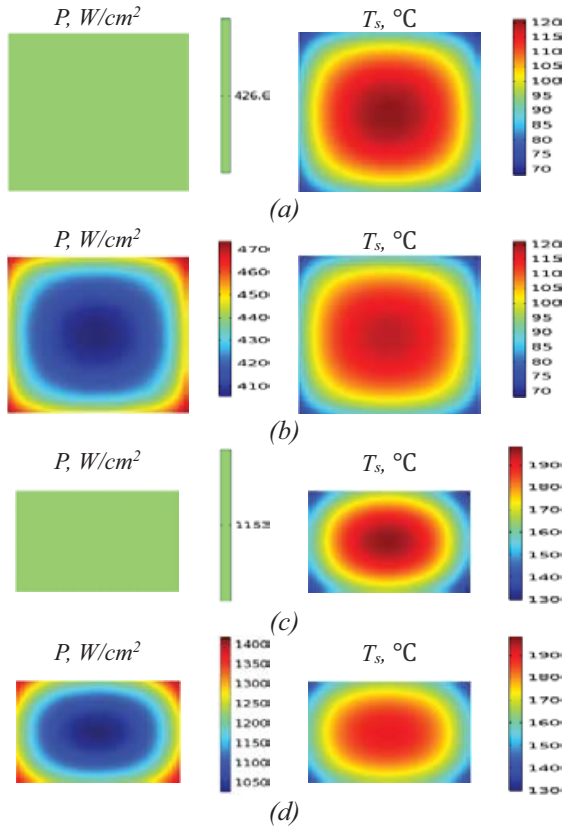


*Figure 8: Top surface distribution of steady-state power density, $\rho_P(x,y)$, and temperature, $T_s(x, y)$, for a total heat of 300 W, htc = 100,000 W/(m²·K), and $T_a$=25 °C: (a) Si IGBT uniform heat dissipation, (b) Si IGBT non-uniform heat dissipation, (c) SiC MOSFET uniform heat dissipation, (d) SiC MOSFET non-uniform heat dissipation'*

*Table 2: Steady-state temperature details of Si IGBT and SiC MOSFET dies for uniform and non-uniform dissipations of 100 W, 200 W, and 300 W (reference: uniform cases)*

| Die type | Power dissipation type | Total power, W | Spatial $T_{min}$, °C | Error, % | Spatial $T_{max}$, °C | Error, % | Spatial ΔT, °C | Error, % |
|---|---|---|---|---|---|---|---|---|
| Si IGBT | Uniform | 100 | 39.6 | 0 | 56.8 | 0.3 | 17.2 | 1.2 |
| | Non-uniform | | 39.6 | | 56.6 | | 17.0 | |
| SiC MOSFET | Uniform | | 60.1 | 0.7 | 82.4 | 0.8 | 22.3 | 4.9 |
| | Non-uniform | | 60.5 | | 81.7 | | 21.2 | |
| Si IGBT | Uniform | 200 | 54.1 | 1.1 | 88.5 | 1.0 | 34.4 | 4.4 |
| | Non-uniform | | 54.7 | | 87.6 | | 32.9 | |
| SiC MOSFET | Uniform | | 95.2 | 2.0 | 139.7 | 1.7 | 44.5 | 9.7 |
| | Non-uniform | | 97.1 | | 137.3 | | 40.2 | |
| Si IGBT | Uniform | 300 | 68.7 | 2.0 | 120.3 | 2.0 | 51.6 | 7.4 |
| | Non-uniform | | 70.1 | | 117.9 | | 47.8 | |
| SiC MOSFET | Uniform | | 130.4 | 3.3 | 197.1 | 3.3 | 66.7 | 17.1 |
| | Non-uniform | | 135.2 | | 190.5 | | 55.3 | |

In this section, a transient study is done to obtain temperature waveforms and evaluate the effect of the temperature-dependent power dissipation on the lifetime calculation. For this purpose, a 300 W pulsed power with 1 Hz frequency is applied to the devices' die, then temperature profiles are found in the center point of the dies' junction where the maximum temperature is typically observed (see Fig. 9).

Actually, when calculating the lifetime, one should consider several points of the die and then select one point with the highest temperature fluctuation. Since during the power-off period, the die temperatures all fall down to the ambient temperature $T_a$ = 25 °C, though, the center point of the die top side is selected.

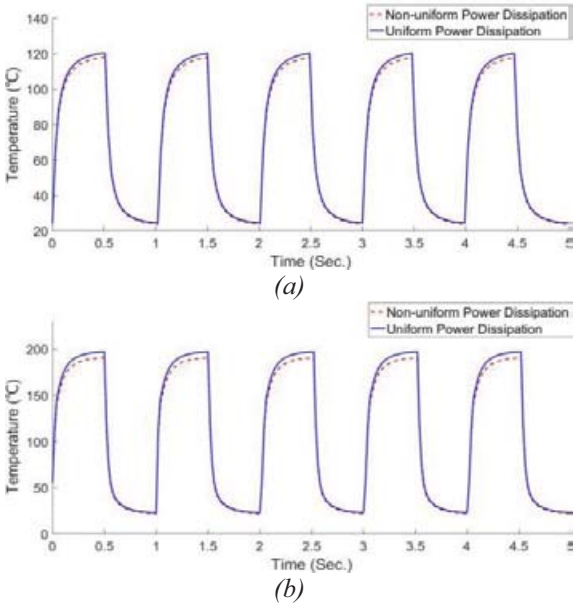


*Figure 9: Transient temperature at 300 W for different power dissipations (a) Si IGBT (b) SiC MOSFET*

*Table 3: Si IGBT and SiC MOSFET lifetime estimates for different power dissipations of 100 W, 200 W, and 300 W (reference: uniform cases)*

| Die type | Power dissipation type | Total power, W | Estimated lifetime, cycles | Error, % |
|---|---|---|---|---|
| Si IGBT | Uniform | 100 | 15,741,000 | 2.7 |
| | Non-uniform | | 16,172,000 | |
| SiC MOSFET | Uniform | | 1,014,700 | 6.4 |
| | Non-uniform | | 1,079,500 | |
| Si IGBT | Uniform | 200 | 604,000 | 7.7 |
| | Non-uniform | | 650,610 | |
| SiC MOSFET | Uniform | | 19,866 | 14.4 |
| | Non-uniform | | 22,724 | |
| Si IGBT | Uniform | 300 | 62,445 | 16.4 |
| | Non-uniform | | 72,695 | |
| SiC MOSFET | Uniform | | 1,238 | 32.8 |
| | Non-uniform | | 1,644 | |

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According to (2) and temperature data as shown in Fig. 9, the end-of-life has been calculated, which is listed in Table 3. It is found that when considering the effect of the temperature-dependent power loss, the lifetime estimation is increased by approximately 16.4% for Si IGBT and 32.8% for SiC MOSFET.

## 7 Conclusion

In this paper, we used Si-IGBTs and SiC-MOSFETs as case studies. It is shown that considering a uniform heat dissipation may result in miscalculation of junction temperatures. It is found that considering the power density distribution affected by the temperature, leads to reducing the maximum temperatures within the die and the temperature difference from the center to the corner of the die as compared to the uniform power dissipation. Thereby, the effect increases the end-of-life calculation. Therefore, investigating temperature-loss interactions is critical in thermal models, especially of high-power-density SiC devices. This concept brings a great benefit to modifying better the results of thermal models developed for temperature stresses and thermal lifetime estimations.

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