Enhancement of Thermo-mechanical Behavior of IGBT Modules through Engineered Threshold Voltages

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Keywords

«Device modeling», «Emerging technology», «IGBT», «Thermal design», «Thermal stress»

Abstract

In this paper, a purposely-imbalanced current density distribution in insulated-gate bipolar transistor (IGBT) chips is introduced to reduce the surface temperature inhomogeneity of standard chips technology. The idea is implemented by modifying the gate threshold voltage across the active chip area, to counteract the uneven temperature distribution of a standard IGBT chip. Coupled thermo-mechanical analysis realized by finite element method (FEM) is used for validating the engineered IGBT chip via comparing different layouts.

Introduction

Insulated-gate bipolar transistors (IGBTs) are key components in a wide variety of high-current applications, like electric vehicles, motor drives, trains, and so on. However, the power handling capability is limited by the maximum operating chip (junction) temperature, which is maximally 175 °C for a silicon-based IGBT [1]. In power modules, the IGBT chip and underlying layers suffer from different coefficients of thermal expansion (CTEs). The CTE mismatch combined with high operating temperature average and fluctuation has been known as the major factor behind thermal stress [2], which can finally lead to IGBT fatigue or failure [3]. Furthermore, the ongoing trends towards planning on smaller device scales beget higher current density per the IGBT chip, which in turn, demand an efficient thermal management to improve the useful lifetime. Therefore, exploring advanced thermal management techniques to improve the efficiency and/or reliability of the IGBT devices has become of great significance in power electronics converters.

Effective device cooling has been known as a solution to the problem by enhancing the heat removal from the device. For example, it was found that, if the cooling effectiveness for a three-phase inverter increases from 50 W/cm^2 (typically a forced air cooling) to 120 W/cm^2 (typically an efficient liquid cooling), the inverter's output current can double from 40 to 80 A/cm^2 [4]. In addition, compared with traditional cooling systems, direct state-of-the-art cooling systems based on sprays, micro-channels, and jet impingements can attain a much higher heat transfer coefficient (HTC) if they can be integrated properly with the semiconductor device packaging technology [5]. For example, it was demonstrated that water submerged jet is capable of delivering cooling capability above 125,000 W/m^2·K [6].

Fig. 1 displays a typical architecture of power IGBT module package with a baseplate. Table I lists the material thermal properties and thickness of the layers of the IGBT package, extracted from Infineon

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IGBT power module rated at 75 A/1200 V (module: IFS75B12N3E4 [7], chip: IGC70T120T8RM [8]). In this configuration, the silicon IGBT chip is soldered onto a direct-bonded copper (DBC) substrate by Sn3.0Ag0.5Cu (SAC305) lead-free solder. The substrate ensures electrical insulation and heat conduction with the help of an alumina (Al_2O_3) ceramic sandwiched between thin copper layers. The DBC substrate is then connected to the copper baseplate with another solder layer.

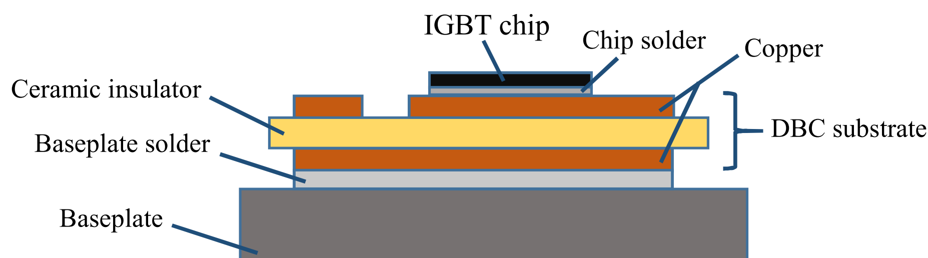

Fig. 1: Typical IGBT module architecture

Table I. Material layers' thermal properties and thickness in the IGBT package

Layer	Thickness [µm]	Density [kg/m^3]	Thermal conductivity [W/(m·K)]	Specific heat capacity [J/(kg·K)]
Si chip	120	2329	148	705
Chip solder- SAC305	100	7800	57	220
DBC	300	8960	401	385
Al_2O_3 ceramic	380	3965	37	785
Baseplate solder- SAC305	250	7800	57	220
Copper baseplate	3000	8960	401	385

Fig. 2 shows the temperature profile at thermal equilibrium along diagonal trace for the typical layout of a simulated IGBT package where the chip is heated with 150 W. In addition, an effective HTC varying from 20,000 - 80,000 W/(m^2·K) is interfaced with the backside of baseplate at the working fluid temperature of 20 °C. It can be found that the HTC rise will reduce the chip temperatures, but the temperature inhomogeneity of 28 °C does not undergo a significant change in effect of the HTC rise. The asymmetry in the profile - slightly higher temperatures at the left-hand side of profile than at the right-hand side - can be explained by a larger heat spreading substrate around colder corners in comparison to the substrate at the end of hotter corners (see Fig. 3). In addition, it was demonstrated that the larger the power loss density, the more significant the temperature inhomogeneity [9].

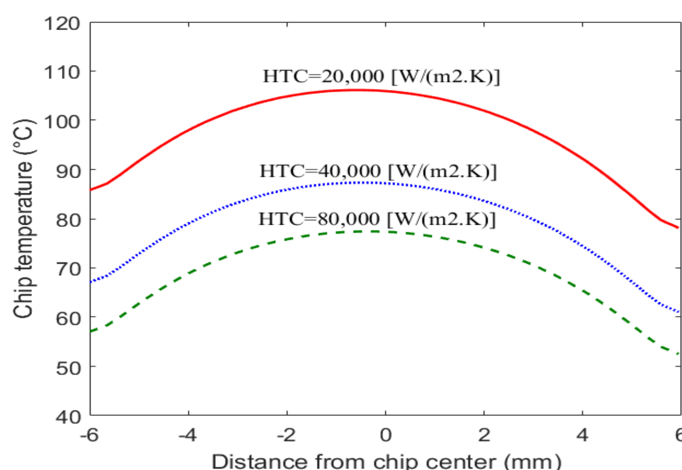

Fig. 2: Temperature profile in thermal equilibrium along diagonal trace on top surface of the typical IGBT chip (the whole chip is considered as an active area)

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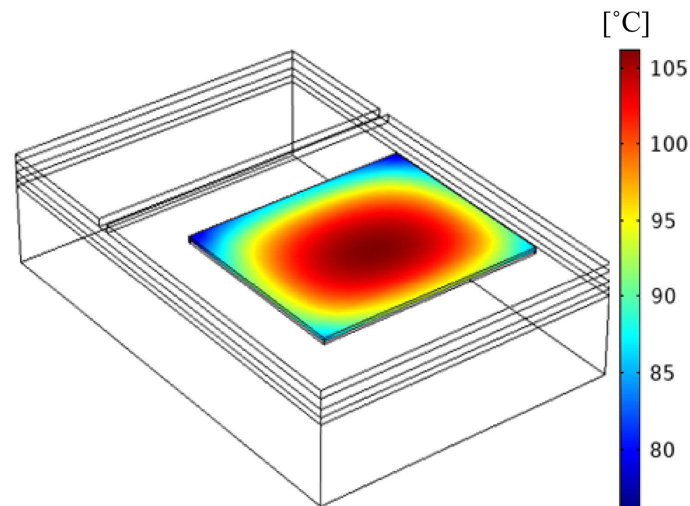

Fig. 3: Surface temperature distribution on an IGBT chip mounted on a multilayer substrate for a power dissipation of 150 W and an HTC of 20,000 W/(m^2·K)

Accordingly, it is found that high HTC cooling solutions designed for the thermal management of the entire IGBT module cannot reduce the temperature inhomogeneity on the individual IGBT chips. This might be logically explained by the fact that the surface temperature inhomogeneity is mainly impressed with lateral heat spreading determined by lateral dimensions of the material layers, while an improvement in the cooling capability is efficient to significantly change the vertical heat spreading of devices, only.

The temperature inhomogeneity is an important topic that is rarely addressed in the literature. It may accelerate the device degradation by creating unbalanced thermo-mechanical stress on critical components, such as solder joints [10]. Also, it may bring along significant errors in maximum junction temperature estimated by temperature sensitive electrical parameters (TSEPs) [11].

To reduce the temperature inhomogeneity, a thermoelectric cooler (TEC) embedded in a layer of the thermal stack was proposed [1]. This localized technique would isothermalize the chip, but it brings along additional complexity, manufacturing cost, power consumption, and new reliability issues in practice.

This paper introduces a novel approach based on a purposely-imbalanced electric current density distribution across the IGBT chip's active area with the target of reduction in the IGBT chip's temperature inhomogeneity. In the next section, how to get such a current density distribution in the active chip area will be described.

Furthermore, in the literature, the whole chip is considered as active area, so that the effect of the presence of inactive gate pad and termination area was neglected. This introduces errors in the thermo-mechanical estimations obtained from modeling, because a more extensive area has been assigned for power dissipation, which in turn, causes smaller power loss density over the chip. Therefore, this paper studies the thermo-mechanical behavior considering a more realistic active area where both gate path and termination region are excluded [12].

Proposed Chip Design

To study the performance of the proposed design approach, we focus on a single-IGBT chip structure, which is cut from a commercial power module, as shown in Fig. 4. This structure contains 5μm-thick emitter aluminum pads with a gate pad at the chip's center and a 500μm-wide termination, which surrounds the active area of 53.4 mm^2. Bond wires have been removed from the IGBT package geometry under study, because they can slightly affect on the thermal results. In the meantime, the cooling system is simplified as a temperature of 20 °C fixed at the backside of baseplate, which accounts for an ultra high heat flux cooling system. Thermal properties and thickness of material layers are the same given in Table I.

 ISBN: 978-9-0758-1531-3 - IEEE catalog number: CFP19850-ART
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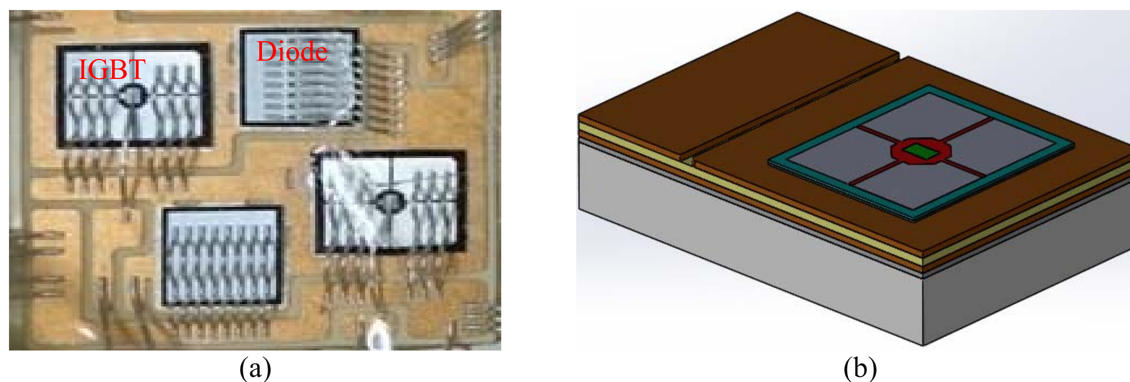

Fig. 4: (a) Real chips in the Infineon IGBT power module (b) Single-IGBT chip package under study

Fig. 5 shows a temperature contour map on the standard chip resulting from injecting a thermal power of 150 W into it. As can be seen, regions near to the chip center have high temperatures while the edges and corners experience low temperatures. Comparison of this contour map with that one shown in Fig. 3 can show the effect of excluding inactive areas of the chip, although there would be an asymmetry in the temperature distribution, yet. Given that the temperature contours are similar to elliptic paraboloids, we propose that the active area becomes split up into a few oval regions where the electric current densities (or power loss densities) counteract the uneven temperature distribution of the standard chip. A design of the engineered IGBT chip with three separated active regions is shown in Fig. 6. Accordingly, larger electric current density is injected into the outer active region while the inner active region bears lower current density. Such different current densities can be realized by calibrating the corresponding gate threshold voltage (V_{th}) through process parameters, such as oxide thickness, amount of charge in the oxide, p-well doping level, and so on [13]. Actually, when changing the parameter V_{th}, the collector current to gate-emitter voltage (V_{GE}-I_C) transfer characteristic would be horizontally shifted as shown in Fig. 7. Similar shifts are also expected for the collector-emitter voltage to collector current (V_{CE}-I_C) output characteristic.

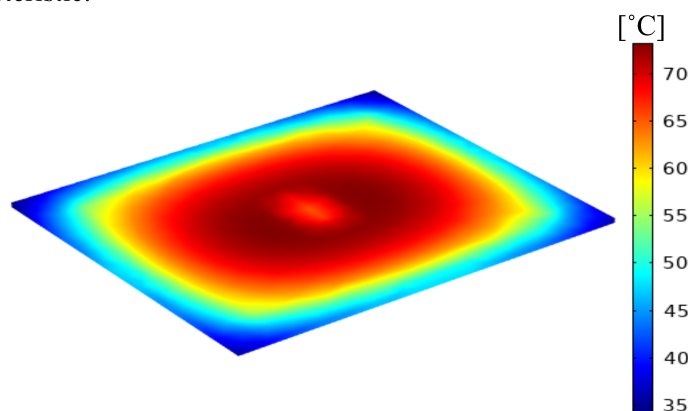

Fig. 5: Temperature contour map of the IGBT standard chip heated with 150 W where the baseplate is fixed at 20 °C

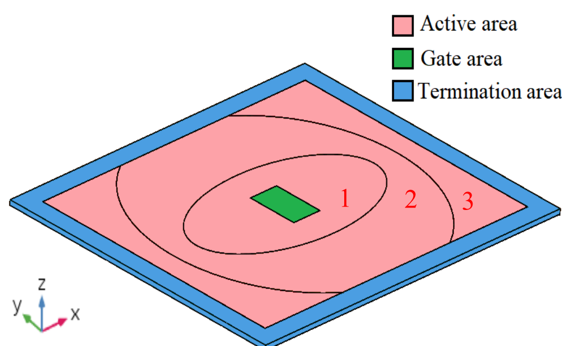

Fig. 6: A 3-D view of the engineered IGBT chip split up into three active regions

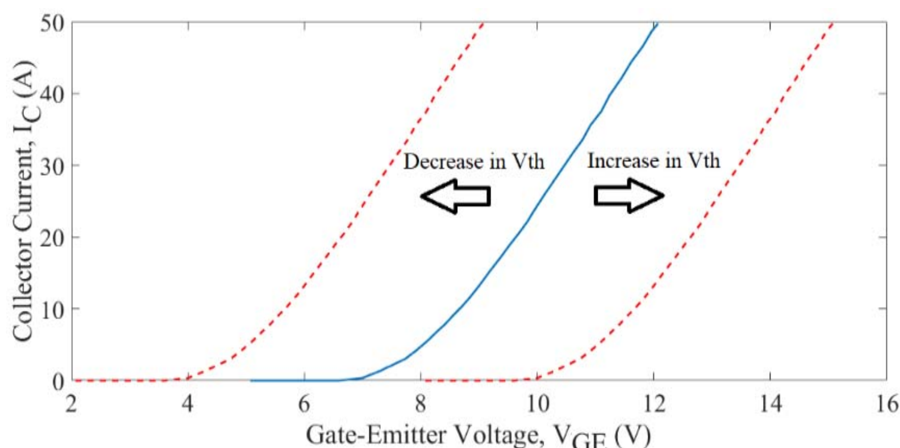

Fig. 7: The effect of the shifted parameter V_{th} on the V_{GE}-I_C characteristic

Threshold Voltage-Electric Current Relationship

Fig. 8 shows a linear region of V_{CE}-I_C output characteristics from the datasheet [7] for the selected IGBT device. This linear region entails an operation in a relatively low V_{CE} while an external voltage of 15 V is applied to the gate-emitter (V_{GE}). Note that the output characteristics are temperature-dependent. In the linear region, the output electric current can be approximated by a linear relationship given as:

$$I_C = K[(V_{GE} - V_{th})V_{CE}] \quad (1)$$

where, K is an inherent constant of IGBT chip.

By fitting Eq. (1) with one of V_{CE}-I_C characteristics at specific junction temperature (T_j) and V_{CE} values, and then extending it to a new temperature with the help of temperature sensitivity analysis, one can estimate the parameter K and, as a result, reach the current I_C in terms of the term V_{GE} (= 15 V) - V_{th}.

Temperature results achieved by the finite element method (FEM) in COMSOL demonstrates that the IGBT chip at the operational condition I_C = 75 A and V_{CE} = 2 V (thermal power $P = I_C \times V_{CE}$ = 150 W) experiences a maximum junction temperature ($T_{j,max}$) about 75 °C, which is the desired temperature. Table II lists the output current density at some V_{th} values for the electro-thermal condition under consideration.

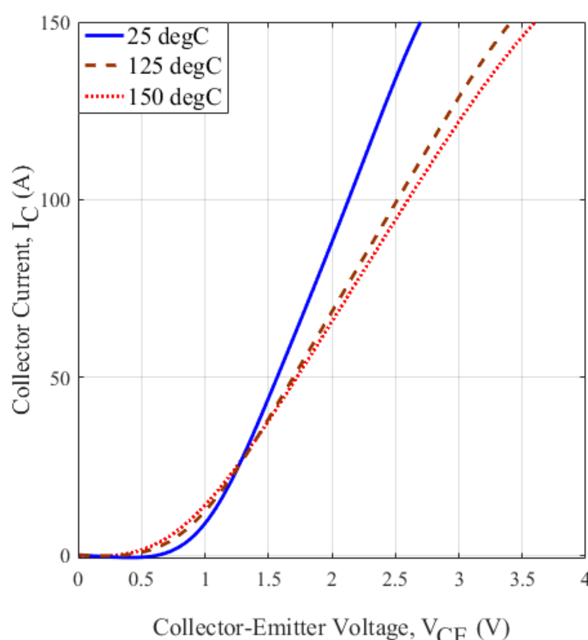

Fig. 8: Temperature-dependent V_{CE}-I_C characteristics of the selected IGBT device [7]

Table II. Electric current density at different V_{th} values (V_{GE} =15 V, V_{CE} = 2 V, T_j = 75 °C)

V_{th} [V]	1	2	3	4	5	6	7	8	9	10
I_C [A]	108.3	104.5	94.8	88.0	81.2	74.4	67.7	60.9	54.1	47.4
Current density, dI_C [A/cm^2]	202.8	195.8	177.5	164.8	152.1	139.4	126.7	114.1	101.4	88.7

Mechanical Model

To study the effect of the proposed chip design on the device reliability, a thermal stress analysis is also performed. In the mechanical modeling, all materials are assumed isotropic and perfectly clamped with elastic properties as given in Table III.

Table III. Material layers' elastic properties in the selected IGBT package [14-15]

Material	Young's modulus [GPa]	Poisson's ratio	CTE [ppm/K]
Aluminum	68.9	0.33	20
Silicon	129	0.28	2.7
SAC305	47	0.36	21.6
Copper	138	0.34	16.8
Alumina	370	0.22	6.3

FEM Simulation Results

In actual practice, the temperature and stress fields are coupled as indicated in Fig. 9. Therefore, a direct thermo-mechanical coupling was established by the COMSOL software with the help of its Multiphysics feature. For mechanical boundary conditions, the nodes at the backside of baseplate were fixed thoroughly, maintaining free all other parts of the package.

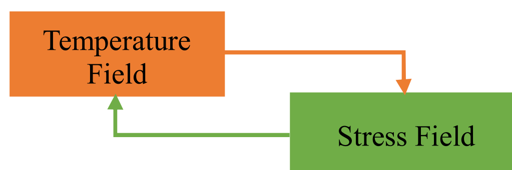

Fig. 9: Coupled multiphysics behaviors in the study

To compare the performance of the package under different chip designs, the total collector current of 75 A is forced to the IGBT chips, which reveal the same on-state voltage V_{CE} = 2 V for that. By using data given in Table II and applying step-function electric currents to the IGBT chip's active area, many trials were done and finally three of the best designs from the viewpoint of maximum surface chip temperature were selected. The electrical information for these engineered designs is given in Table V.

Table V. Electrical parameters of active regions in the standard chip and engineered chip

Design	Active region	V_{th} [V]	Current density [A/cm^2]	Power loss [W]
Standard	1,2, 3	5.9	140.4	150.0
Proposed-1	1	10.6	81.0	19.3
	2	4.6	157.1	83.0
	3	4.6	157.1	47.5
Proposed -2	1	9.1	100.1	23.8
	2	6.1	138.1	72.9
	3	3.1	176.1	53.3
Proposed -3	1	7.6	119.1	28.3
	2	7.6	119.1	62.9
	3	1.6	195.1	59.0

As expected the outermost active region carries a larger current density requiring a smaller V_{th} value in comparison to the innermost region. The temperature contour maps in Fig. 10 demonstrate that the engineered chips produce a smaller temperature inhomogeneity with smaller maximum temperatures (at center region) and larger minimum temperatures (at edges) than those of the standard chip. Fig. 11 also presents temperature profiles along the diagonal trace of the IGBT chips' top surface. Also, the detailed thermal results are given in Table VI. It can be found that the standard chip has a maximum temperature of 73.7 °C, but it is decreased in the second design of engineered chip to 68.1 °C, that is decreased by 7.6 %.

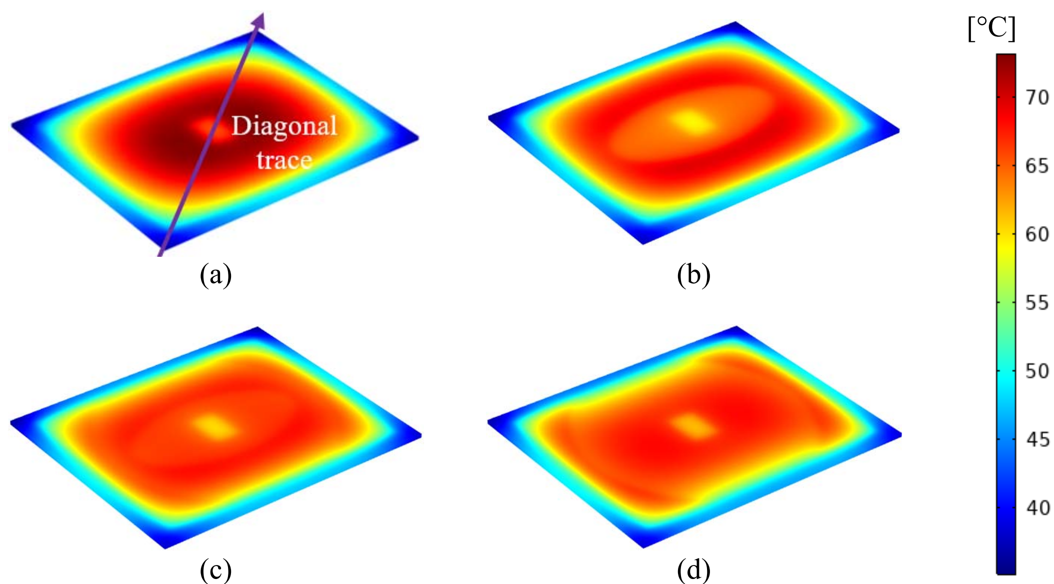

Fig. 10: Temperature contour map of IGBT chip with (a) standard design, (b) engineered design 1, (c) engineered design 2, and (d) engineered design 3

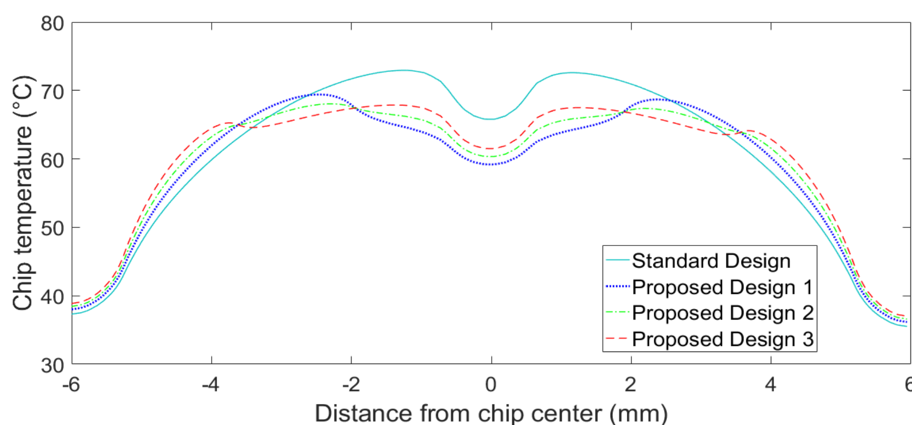

Fig. 11: Temperature profile along diagonal trace of standard and engineered chips

Table VI. Detailed temperatures for the standard and engineered chips

Chip design type	Maximum temperature [°C]	Minimum temperature [°C]	Temperature difference [°C]
Standard design	73.7	34.2	39.5
Engineered design 1	69.9	34.8	35.1
Engineered design 2	68.1	35.1	33.0
Engineered design 3	68.4	35.4	33.0

To study the reliability of device with the proposed chip designs, thermal stress at the chip solder joint, where the most common failures often occurs in real applications, is investigated. Fig. 12 shows the stress distribution at the solder layer joint for the standard and engineered chips. It is found that the engineered chips can make more uniform stress on the solder joint with a smaller maximum stress by 11.8% compared to the standard design. This means that the engineered IGBT chip can improve the reliability and opeartional lifetime of the IGBT device.
Furthermore, the effect of the proposed approach in the device's lifetime is investigated in this way that electric current pulses as large as 75 A in total are injected at a frequency of 1 Hz and a duty cycle of 50%. Fig. 13 shows the temperature profiles at a point on the chip surface (near to the gate pad) that experiences the largest temperature among all at every time of simulation. It is found that the proposed approach is also effective in reducing the peak temperature in transient conditions.

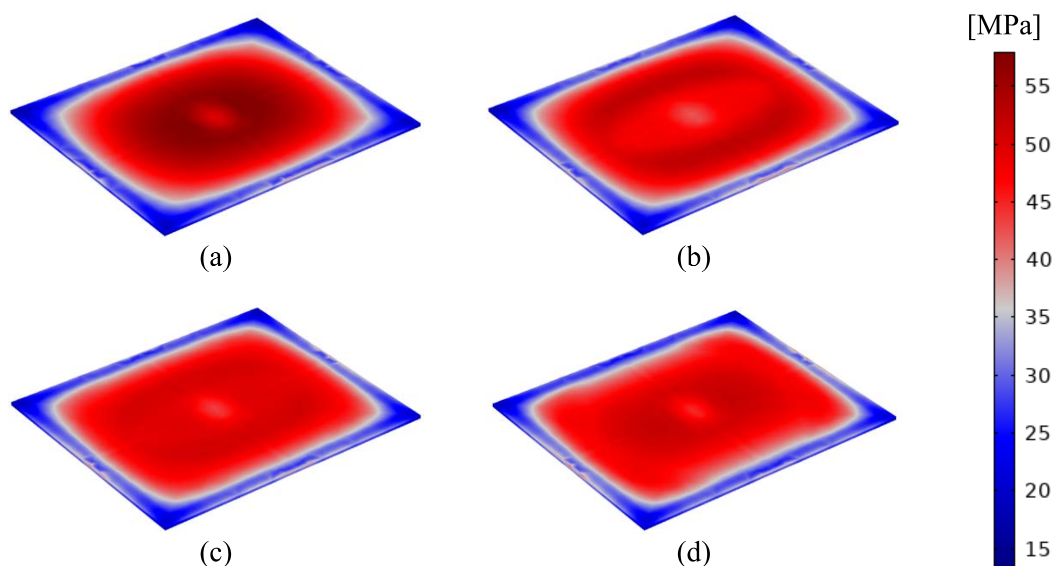

Fig. 12: Stress contour map of IGBT chip with (a) standard design, (b) engineered design 1, (c) engineered design 2, and (d) engineered design 3

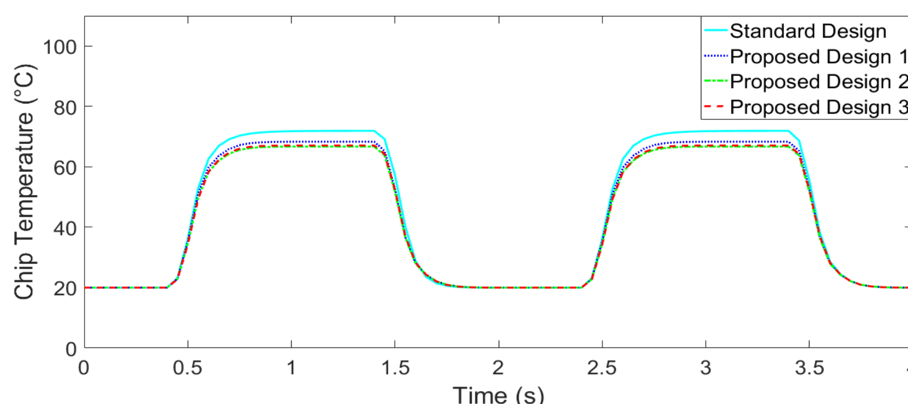

Fig. 13: Temperature profile on a point of standard and engineered chips' top surface (the point experiences maximum temperature at every moment of the simulation time)

In order to study the effect of peak temperature decreased in the engineered chip on the reliability lifetime, the Bayerer model is adopted [16] as below:

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot e^{\beta_2/T_j} \cdot t_{on}{}^{\beta_3} \cdot I^{\beta_4} \tag{2}$$

where ΔT_j is swing of surface temperature per power cycle, t_{on} is power-on-time, I is current per wire of chip, K is Arrhenius factor, and parameters β_1 to β_6 are constants defined as $\beta_1 = -3.483, \beta_2 = 1.917 \times 10^3$, $\beta_3 = -0.438$, $\beta_4 = -0.717$, which well fit with Infineon IGBT modules [16].
By applying the temperature profiles of Fig. 13 to Eq. (2), the lifetime is calculated 57% longer for the third engineered design in comparison to the standard design.

Conclusion

In this paper, a new technique to reduce the surface temperature inhomogeneity of an IGBT chip is introduced, in which the active chip area is split into three regions carrying different electric current densities. FEM results verify the performance of the proposed approach, which yields a perceptible reduction either in temperature variation or maximum temperature of IGBT chip surface. As a consequence, the thermal stress magnitudes at the underlying layers can be reduced and, as a result, the system reliability will be improved. It is shown that the improved design may reduce maximum chip temperature up to 7.2%, reduce maximum thermal stress of the chip solder joint up to 11.8%, and increase lifetime up to 57%. Furthermore, being the maximum temperature reduced in the proposed approach, the gained budget can alternatively be used to increase current capability. It is necessary to mention that the proposed approach can even further improve the efficiency and reliability of the power device if the active area is split up into a larger number of regions experiencing different V_{th} values.

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