A Multi-Layer RC Thermal Model for Power Modules Adaptable to Different Operating Conditions and Aging

M. Akbari[a], A.S. Bahman[b], M.T. Bina[a], B. Eskandari[c], F. Iannuzzo[b], F. Blaabjerg[b]
[a]K.N. Toosi University of Technology, Tehran, Iran
[b]Aalborg University, 9220 Aalborg, Denmark
[c]Malayer University, Malayer, Iran
E-mail: mohsen.akbari.eng@gmail.com

Keywords

Abstract

Semiconductor devices are often the most vulnerable components of power electronics converters among which thermal failures are the most likely ones. Thus, more accurate but straightforward thermal models are needed to efficiently do actions such as lifetime prediction, thermal management, etc. This paper presents a Foster-type equivalent transient thermal model developed through finite element simulations for a commercial Si IGBT power module. Such thermal models can easily merge into circuit simulation programs and even can be employed as real-time temperature estimators. However, fixed thermal models may give large errors in different operating conditions. In addition, they become unable to satisfactorily estimate temperatures over time, because of the thermal aging phenomenon. Thus, in this study, the thermal model of the power module is developed to be adapted to different boundary conditions - ambient temperature, and cooling system – as well as thermal aging of solder joints, which is the most common failure in the power modules. Also, the thermal model features the effect of power loss, and the cross-coupling effect among nearby semiconductor dies. Comparisons with FEM verify the performance of the studied thermal model.

Introduction

Today, power converters have a critical functionality for the control and conversion of the electric power in applications such as renewable energy generation, automotive electronics, and consumption so that the occurrence of any failure in them can lead to the suspension of the desired process and even significant cost. Accordingly, improving the reliability of the power converters at the design stage is of great importance to engineers. In [1] it is reported that among power converters' components, semiconductor devices are considerably vulnerable among which steady state and cyclical temperatures are reported as stressors for more than half of failures [2]. Therefore, most of the researches on semiconductor devices'reliability have been focused on the thermal analysis. For example, to predict the lifetime of semiconductor devices, a well-known equation called Coffin-Manson-Arrhenius law is:

$$N_f = \beta \times \left(\Delta T_j\right)^{-\alpha} \times exp\left(\frac{E_a}{k_B \times T_{jm}}\right) \tag{1}$$

where N_f is the number of cycles to failure, ΔT_j is the junction's temporal temperature fluctuation (where power losses are converted to the heat), T_{jm} is temporal mean temperature, E_a is activation energy, k_B is Boltzmann constant, β and α are empirical parameters.

Moreover, one can employ junction temperature of the semiconductor devices in control systems. In such active thermal controllers, on-line measured temperatures are applied to regulate the power loss in a power module, e.g., through switching frequency regulation [3], and advanced modulation schemes [4], or among parallel converters, e.g., through power-sharing [5], and reactive current circulation [6].

To find the junction temperature, several experimental techniques, which employ temperature-sensitive electrical parameters (TSEPs) are introduced in the literature, e.g., the on-state collector-emitter voltage drop ($V_{CE,ON}$) at high electric current levels [7]. However, TSEP-based methods provide a temperature of the junction, only, and also between the minimum and the maximum temperatures [8]. Note the device temperature is very non-uniformly distributed. In addition, TSEP-based methods often employ a

complex measurement circuit and also reduce the efficiency of power devices. Even, one may use an infrared (IR) camera [9] or optical fibers [10] to map the surface temperature distribution of power devices. However, they need to be decapsulated which is not possible in real applications. In addition, note since some thermal failure mechanisms happens in layers other than a junction, the temperature of those layers also becomes essential from the reliability standpoint. But, the above approaches are unable to provide such temperature of layers, e.g., solder joints.

To overcome aforementioned limitations, modeling and simulation of power devices by means of computer programs are applied in some research works. Thermal models can typically be classified into two types. One way is the use of numerical methods, e.g., finite element method (FEM), finite difference method (FDM), and finite volume method (FVM) [11]-[13]. All three methods, which can model complex geometries, are being employed in most current commercial computer programs. For example, COMSOL Multiphysics, ESATAN, and ANSYS Icepak, providing thermal results, are based on FEM, FDM, and FVM, respectively. Although FDM gives the least acceptable approximate for the least computational time, FVM enables best approximate with highest computational time. In this study, COMSOL Multiphysics has used in which FEM provides a fair approximation with a reasonable computational time. Nevertheless, it still suffers from the high computational time for on-line temperature measurements, especially when large time constants, such as a heatsink, is present.

Another type of thermal models is lumped resistor-capacitor (RC) networks, which provides much less computational time. An advantage of RC networks is that they are simple and easy to be implemented in any electronic circuit simulator such as PLECS, and SPICE. RC networks are classified into Foster and Cauer types. Foster thermal network parameters can be extracted from devices' transient thermal impedances obtained from numerical methods or field measurements. But Cauer thermal network parameters are determined by the knowledge of the physical structure of devices. Fig. 1 shows a schematic of these thermal networks. In both thermal networks, power loss dissipated in semiconductor devices and the ambient temperature emerge as a current source and a voltage source, respectively. Middle points in the Foster ETNs often do not have physical meaning, while they represent the temperature of corresponding internal layers of devices in the Cauer ETNs. In addition, it is worth knowing that in Cauer ETNs, the thermal path is defined as one-dimensional (1-D) and the thermal coupling effect among nearby dies can be hardly considered. Thus, temperature estimation errors of Cauer ETNs are more significant when comparing to those of Foster ETNs.
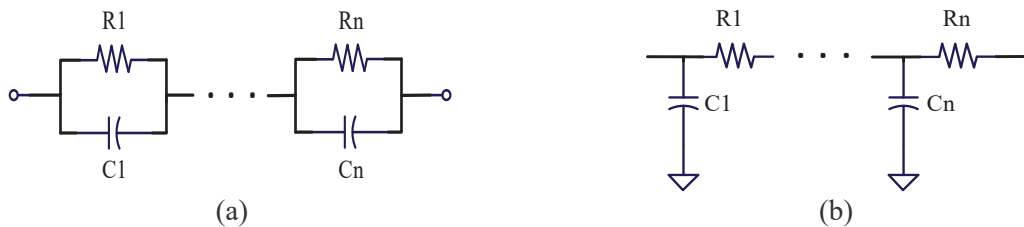

Fig. 1: Typical *n*-order RC lumps-based thermal networks, (a) Foster (b) Cauer

Moreover, in [14] it is presented that when changing the boundary conditions around the power device, - ambient temperature and cooling system - or the power loss input to devices, the accuracy of fixed thermal RC networks is deteriorated. Furthermore, thermal aging of devices can cause to deteriorate such fixed networks over time. Main failure mechanisms are bond wire lift-off and solder joint fatigue, which are often due to sizeable temporal temperature swings and the mismatch of thermal expansion coefficients between interconnections. Bond wire lift-off can raise the device's temperatures through the increased on-state voltage and as a result the increased power loss. However, the solder joint fatigue puts its effect by reducing the area of the thermal path, which increases the thermal resistance and finally the device's temperatures. Note these mechanisms have a coupling with each other and can intensify other. The process of the above mechanisms will continue as long as all bond wires are removed.

The purpose of this study is to estimate temperatures of critical layers in a commercial insulated-gate bipolar transistor (IGBT)-based power module using a Foster ETN developed through FEM simulation in a COMSOL Multiphysics environment, which can be used for the degraded module and adapted to different boundary conditions. Critical layers under study are the semiconductor die, die (solder) joint, direct bonded copper (DBC) substrate, baseplate (solder) joint, and baseplate-to-ambient section.

System under Study

Fig. 2 shows a schematic cross section of the internal structure of power module mounted on the heatsink. As shown in Fig. 2, the semiconductor die is the top layer where the active area or junction, is defined. Also, a ceramic layer to electrically isolate the dies from the baseplate is sandwiched between two copper layers, which make the DBC substrate. In addition, solder joints are used to attach dies to DBC substrate (die joint), and DBC to the baseplate (baseplate joint). Moreover, since the surfaces of heatsink and baseplate are rough, a thin layer of thermal interface material (TIM) is inserted between them to fill in gaps and as a result to improve the heat transfer efficiency.

The semiconductor device under study is a silicon (Si) IGBT power module with the part number of IFS75B12N3E4_B31 (1200V/75A) manufactured by Infineon Technologies which is placed on a heatsink by a Si TIM. The power module is a three-phase half-bridge inverter composed of six IGBT dies, and six fast recovery diode (FRD) dies. Fig. 3 presents a picture of this uncovered module. The thickness of applied TIM is considered as 0.1mm, and the heatsink has an area of $30 \times 35 \text{cm}^2$ and 30 parallel fins. Also, a configuration of the numbered dies of the selected power module is shown in Fig. 4 so that we refer to this numbering in the following.

Note, the effect of the coolant is investigated through an equivalent heat transfer coefficient (htc) applied to the heatsink fins and surfaces. The parameter htc between a solid and fluid by convection can generally be defined as:

$$htc = \frac{Q}{\Delta T} \tag{2}$$

where Q is the heat - power loss in the power module - and ΔT is the temperature difference between the solid surface and the fluid area.

The heatsink modeling will be more described in next sections. In addition, the ambient temperature is considered all around the heatsink so that the cooling temperature is assumed as equal to the ambient temperature and natural air convection is defined for the outer surfaces of the heatsink.
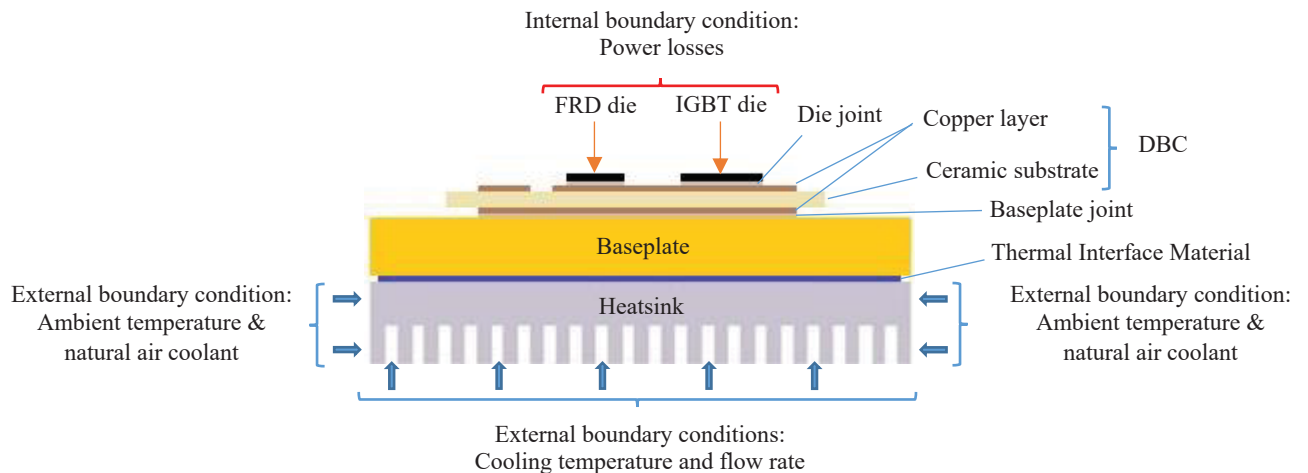

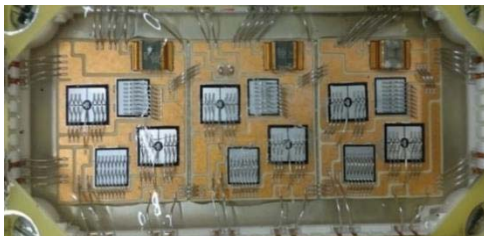Fig. 2: Internal structure of IGBT module and boundary conditions

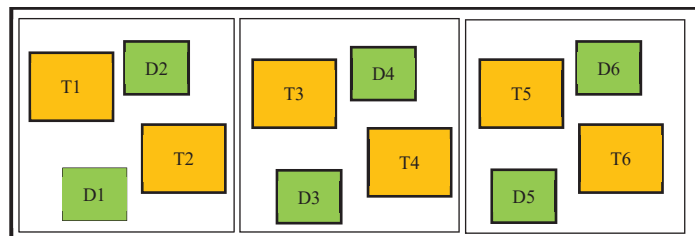Fig. 3: An image of inside the selected Si IGBT module

Fig. 4: The configuration of the semiconductor dies in the selected IGBT module, T: IGBT, D: FRD

It should also be mentioned that a scanning electron microscope (SEM)-based technique has been used to find thicknesses and materials of constituent layers. An example of these measurements has been shown in Fig. 5.
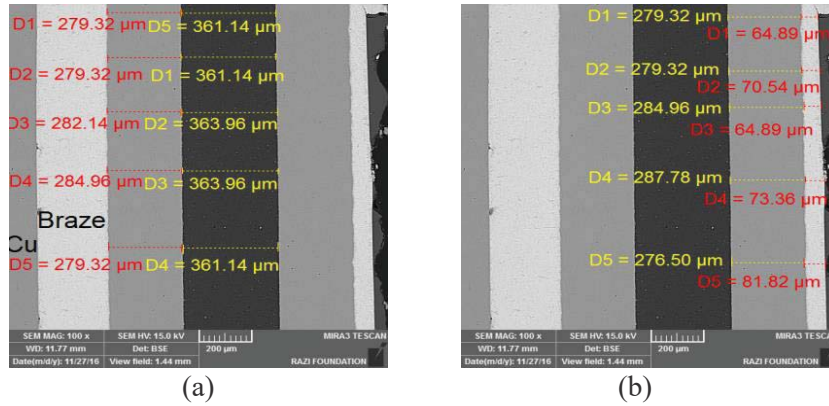
Fig. 5: SEM images, ×100: (a) thickness of DBC's lower copper (red color) and DBC's Al$_2$O$_3$ ceramic (yellow color), (b) thickness of DBC's upper copper (yellow color) and die solder (red color)

Thermal Model

In the literature, different structures of the RC ETNs have been utilized. For example, in some ETNs, heatsink and usually baseplate are shared between different semiconductor dies. In some others, thermal coupling effects between internal layers are ignored. The ETN, which will be employed in this study, is shown in Fig. 6 where no component is thermally shared, and thermal coupling effects are included.
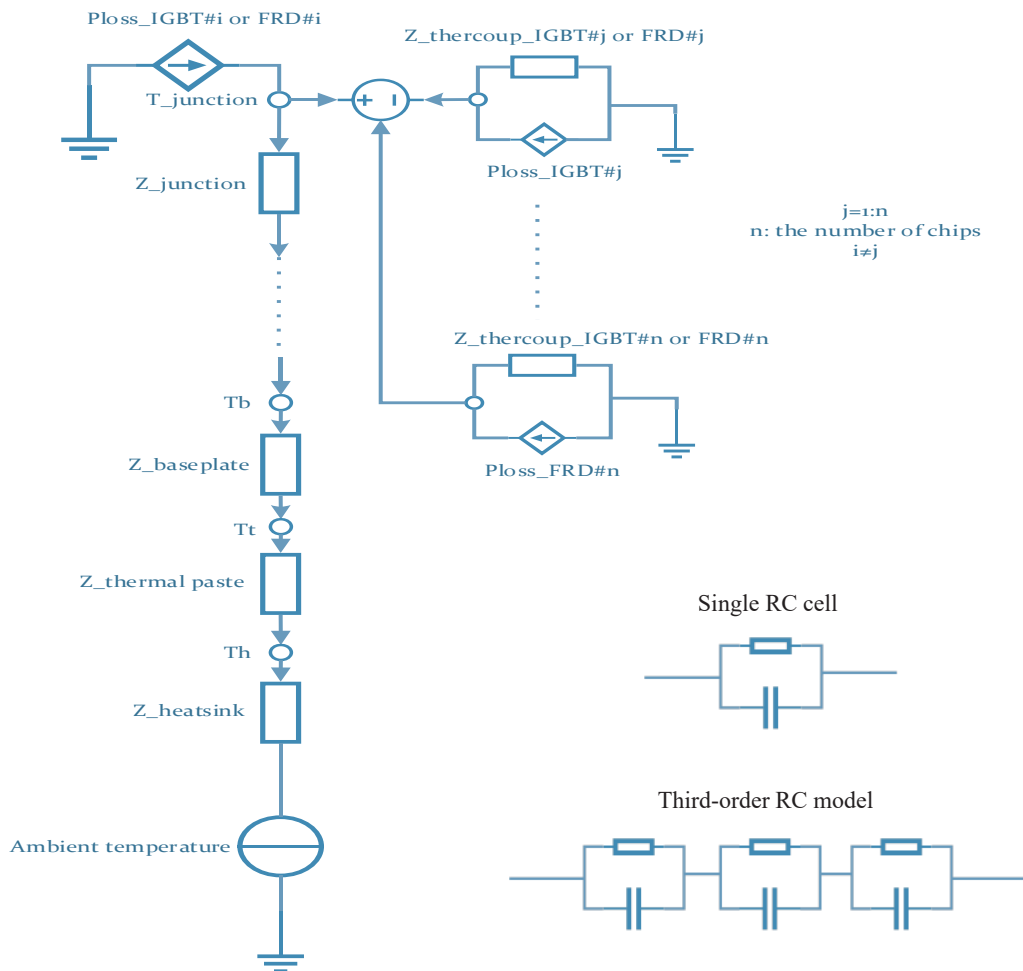

Fig. 6: Foster ETN for the selected system

In addition, it is realized that internal layers of the module - Si die, die joint, DBC substrate, baseplate joint, and baseplate - can be modeled by a single RC cell as shown in Fig. 6. Also, TIM is modeled by a single RC cell. While it is detected the heatsink's effect can be modeled by a third-order Foster model.

Moreover, to adapt the thermal model with different boundary conditions, Si die and DBC substrate are found to be parameterized directly in terms of the ambient temperature (T_a), and power loss (P_{loss}). While RC cells of the heatsink are parameterized inversely in terms of the parameter htc. Furthermore, a third-order model is figured out to present cross-coupling effects among dies whose RC parameters are fixed in different conditions.

Methodology

In [14] it is found that, when a die is heated, then neighbor dies will have a significant temperature rise; the closer the dies to one another, the larger the thermal cross-coupling effect. Therefore, the cross-thermal impedance cannot be ignored in the study.

In this study, the FEM analysis is employed to obtain a transient temperature of layers, and then the corresponding thermal impedance would be mathematically obtained as follows:

$$Z_{i,(n,m)}(t) = \frac{T_{i,n}(t) - T_a}{P_m} \tag{3}$$

where t is time, $Z_{i,(n,m)}$ and $T_{i,n}$ are respectively thermal impedance, and temperature of the ith layer of the nth die when mth die is heated, T_a is the ambient temperature, and P_m is the total average power loss applied to the mth die. If $n=m$, then Z will be self-thermal impedance; otherwise, it will be cross-thermal impedance. To better clarify the concept, in Fig. 7, self-thermal and cross-thermal impedances for a leg of the module shown in Fig. 3 and Fig. 4, which includes two IGBTs and two FRDs, have been depicted.
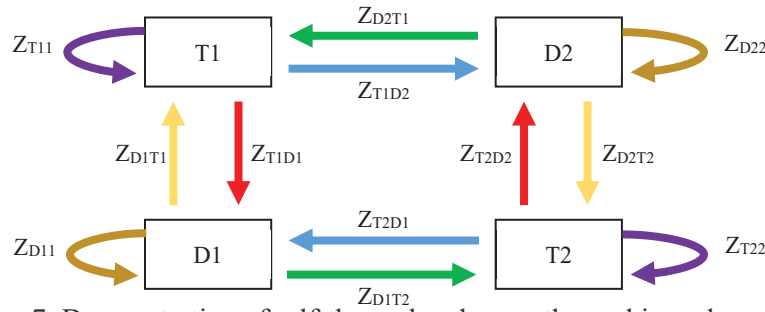

Fig. 7: Demonstration of self-thermal and cross-thermal impedances

After obtaining the thermal impedances using Eq. (3), the Foster network's RC parameters can be determined by a curve fitting technique, which establishes the following mathematical series:

$$Z_i(t) = \sum_i R_i \left(1 - exp\left(-\frac{t}{R_i C_i}\right)\right) \tag{4}$$

where t is time, R_i and C_i are thermal resistance and heat capacitor of the ith cell of the corresponding layer, respectively.

It is worth to point out that accurate meshing is fundamental for FEM simulations. The system has to be subdivided into smaller and simpler parts, called finite elements in FEM. When refining the mesh, the number of finite elements will increase, and in turn, the accuracy will improve despite losing the computational time. In this study, the mesh has been manually optimized through a trade-off between the accuracy and the computational time. In other words, it is refined by predefined options in COMSOL Multiphysics environment as long as thermal results do not change significantly. Accordingly, the power module mounted on the heatsink has been meshed by nearly 250,000 tetrahedral elements in this study (see Fig. 8).
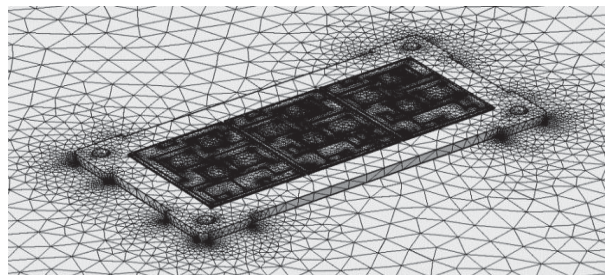

Fig. 8: Finite element-meshed IGBT power module

Temperature Ambient-dependent ETN

Since layers of the module often meet different temperatures during operation, and thermal properties of some constituent materials are sensitive to the temperature, we are faced with a temperature-dependent RC network. The thermal properties of material layers are defined as thermal conductivity and specific heat capacity. Although temperature dependence of thermal properties of pure metals - aluminum and copper - can be negligible, those of Si and Al_2O_3 materials dramatically change with temperature. In Table I, one can find thermal properties of the layers for the selected IGBT module.

Fig. 9 shows thermal impedances of the T1 junction for different ambient temperatures when a fixed P_{loss} is injected to T1, only. One can observe a significant difference between thermal impedance responses at T_a=25°C and T_a=150°C. In [15], errors are reported within 11% for the steady state, i.e., thermal resistance, due to the assumption of the temperature independence for thermal models. In addition, it is found that the most influenced layer is Si die and DBC substrate. Moreover, one can see large time constants for thermal impedances shown in Fig. 9 because of employing a sizeable heatsink which represents a large heat capacity.

Table I: Characteristics of layers for the selected IGBT module

Layer	Material	Density (kg/m³)	Thermal conductivity		Specific heat capacity	
			Temp. (°C)	Value (W/(m·K))	Temp. (°C)	Value (J/(kg·K))
Die	Silicon	2329	25	148	25	705
			125	99	125	788
			225	76	225	831
Solder joints	SnAgCu	7800	all	57	all	220
DBC ceramic	Al_2O_3	3965	25	37	25	785
			125	27	125	942
			225	21	225	1077
Copper	Cu	8960	all	401	all	385

Power Loss-dependent ETN

Fig. 10 shows thermal impedances between the T1 junction and the ambient for different power losses created in T1, only, under a fixed T_a. As shown, one can see a positive correlation coefficient between the thermal impedances and power losses. In [14] it is investigated that the most influenced layer from this standpoint is Si die and DBC substrate. This effect is similar to that of ambient temperature described in the previous section. Because both items affect thermal impedances through variation of temperatures imposed on the layers.

Heat Transfer Coefficient-dependent ETN

The parameter *htc* of four cooling systems has been calculated according to equations provided in [16]. It is worthwhile to say that the fluid characteristics of the inner environment of the heatsink can be variable, while the outer environment of the heatsink is ever surrounded by the natural air of the ambient. The cooling mechanisms are defined as natural air, forced air, natural water and forced water. In Table II, parameter *htc* of forced air and forced water cooling systems have been provided for a specific velocity to show its effect. While, in the parametrization process of RC cells in Foster ETN, a velocity range of 0.5m/s to 10m/s is evaluated. As you can see in Table II, with mutating the fluid from air to the water or from natural convection to forced convection, the parameter *htc* of the internal environment will increase, and that of the outer section will decrease because the improved cooling power of the fluid causes the effect of outer environment to diminish.

Fig. 11 shows the effect of different cooling systems, listed in Table II, on the thermal impedance of the T1 junction when it is heated by 10W, only. One can find that there is a negative correlation coefficient between thermal impedances and parameter *htc*. Because, the thermal resistance of the heatsink with an effective heat transfer area, *A*, is defined based on the parameter *htc* as follows [17]:

$$R_{th,hs} = \frac{1}{htc \cdot A} \tag{5}$$

As concluded from Eq. (5), a higher *htc* due to an improved cooling system gives a smaller $R_{th,hc}$.

Also, it is found that the heatsink is the most influenced section due to the change in the cooling system.

Table II: Parameter *htc* for different cooling mechanisms

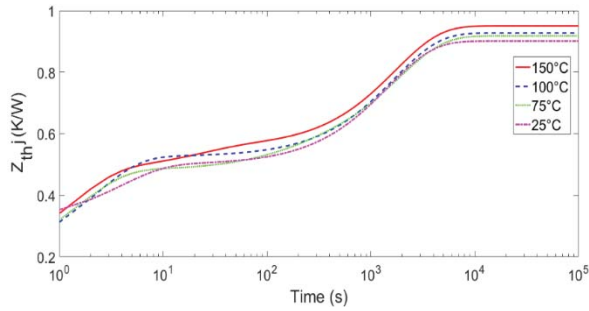| Cooling system	*htc* of the outer environment (W/(m²·K))	*htc* of the inner environment (W/(m²·K))
Natural air	4.7	2.3
Forced air – 6m/s	1.8	11.1
Natural water	1.2	51.2
Forced water – 1m/s	0.6	899.7

Fig. 9: Thermal impedances of the T1 junction at different temperatures for P_{loss}=10W and the natural air cooling system
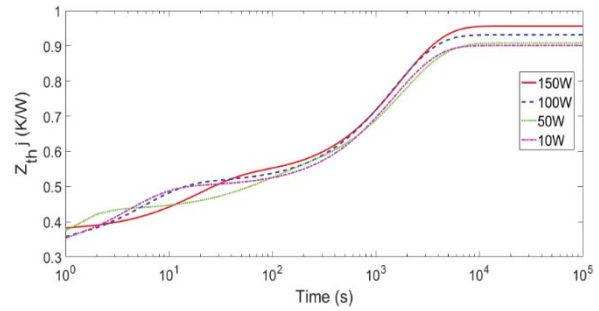
Fig. 10: Thermal impedances of the T1 junction at different power losses for T_a=25°C and the natural air cooling system
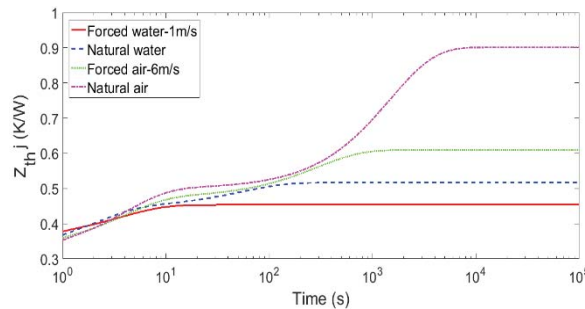

Fig. 11: Thermal impedances of the T1 junction at different cooling systems for T_a=25°C, and P_{loss}=10W

Solder Joint Aging

In [18] it is investigated the fatigue in an Sn-Ag-based solder scarcely emerges in temporal temperature swings of dies (ΔT_j) up to 60°C, while bond wires can wear out in such ΔT_j. However, the solder joint fatigue occurs earlier in the range of ΔT_j greater than 110°C in comparison to the bond wire fatigue. In addition, because of the larger area of the DBC substrate in comparison to that of the dies, the generated heat does not significantly rise the temperature on the baseplate joint. In [19] it is presented that the damage in a baseplate joint is negligibly influenced by ΔT_j up to 100°C or power cycle times below 10s. It is worth knowing that most power modules are operated in a ΔT_j lower than 100°C and power cycle times below 10s is also rarely present in real applications. Consequently, one can conclude that temperature swings from 60°C to nearly 100°C may make damages in the die joint, only. While, in the range of ΔT_j higher than 100°C, the fatigue may appear in both die joint and baseplate joint. It is worth knowing the baseplate joint fatigue can be also caused by ambient temperature variations that has low time constants.

The fatigue mechanism of the solder is as follows. The Sn–Ag-based solder has high yield strength, and cracks do not depend on plastic deformation but on transformation in the solder microstructure, in other words, the grain growth of tin. Most of the Ag existed in Ag_3Sn intermetallic are disseminated like a network around the grain boundaries of the elemental tin. Under thermal stress, these agglomerate and their grain size coarsens, weakening the grain boundaries of tin. Therefore, the grain size of tin also coarsens, and boundary sliding and cavities (grain boundary micro-voids) are generated at the grain

boundaries of tin. These cavities are thought to be the starting points of solder cracks expanding along the grain boundary [18].

Moreover, in [18] it is found that in the case of Sn-Ag-based solder joints, the propagation of cracks is nearly concentric, originating almost directly under the semiconductor die. Therefore, the delamination in which the aging of a solder joint starts from the edges inward rarely appears in Sn-Ag-based joints, and if it is there, the amount is small and can be ignored [19].

As mentioned before, the overall result of voids and/or cracks is to reduce the solder cross-section area, which is existent for the heat dissipation. This eventually leads to an increase in thermal resistance and dies' maximum temperature.

Since voiding is dependent on many factors, which are extremely difficult to control, voids' distribution is random in size, location, and geometry within solder joints. One can find IPC (Institute of Interconnecting and Packaging Electronic Circuits) criteria and/or military criteria about the permissible voids' area. Although the former is not related to rectangular solder joints, the latter can apply to power modules. The MIL-STD-883D, method 2030 [20], requires that the single solder void and overall solder void should not exceed 10% and 50% of the total solder joint area. However, the voids' geometry may not affect the thermal resistance [21]. Therefore, this study employs a circular void approach precisely embedded in the solder joints. Of course, in reality, solder voids do not follow a simple exact orientation but progress chaotically.

Furthermore, voids can be simulated as trapped air (0.0261 W/mK thermal conductivity) or vacuum pockets with no material property. By considering that there is no remarkable variation in the results obtained from the two different approaches. Therefore, to decrease computational times, all cases of void models discussed in this study are modeled as a vacuum pocket.

Given the MIL-STD-883D standard, the overall void area percentages of 5, 10, 20, 30, 40, and 50% are chosen as levels of interests. Note, as mentioned before, single voids' area are limited to 10%. In the case of distributed voids, we have assumed a configuration type of 5×5 of voids in the die joint and baseplate joint of the selected IGBT module as shown in Fig. 12(b). The circular voids area is changed through the radius. Fig. 13 shows the variation of thermal resistance with the overall void area for both single void and distributed voids under the natural water cooling system, T_a=25°C and thermal power of 10W. As shown, with the overall void area rise, thermal resistance increases because the effective area of solder joint that helps transfer the heat is reduced. It is worth knowing that some investigations show the thermal capacitances do not significantly change even in large degradation degrees.

(a)   (b)

Fig. 12: Typical void configurations in the solder joints: (a) single void, (b) distributed voids (5×5)
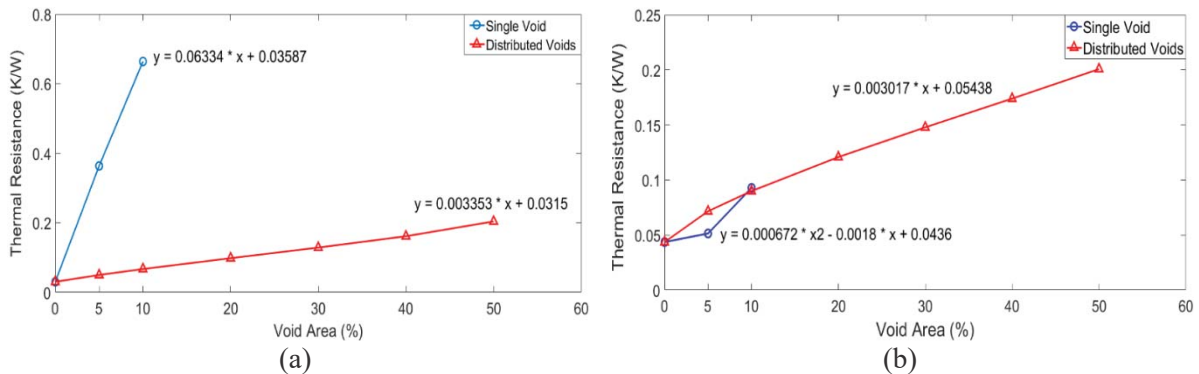

(a)   (b)

Fig. 13: The variation of thermal resistance for different degrees of the solder void area: (a) die joint, (b) baseplate joint

Effects of boundary conditions, power loss, and thermal aging discussed above are included in the ETN through the MATLAB curve fitting toolbox using linear polynomials as below:

$$R_{th} \ or \ C_{th} = \frac{(a \times T_a + b)(c \times P_{loss} + d)(e \times A_{void} + f)}{(g \times htc + h)} \tag{6}$$

where pairs of (a, b), (c, d), (e, f), and (g, h) are parameters obtained for the linearization of the effects of ambient temperature, power loss, overall void area, and the cooling system, respectively.

Simulation Results

In this study, to simulate a real condition, a pulsed power loss of 75W with the frequency of 1Hz and duty cycle of 0.5 is applied to T2 and T3. In other words, we have the power for 0.5s and then the power is off for 0.5s, and this repeats. The parameter T_a=30ºC and natural water cooling system are selected. Also, a 5×5 circular void distribution with 20% overall area is considered in the T2 die joint. Accordingly, maximum temperature at some layers of the power module through the FEM and the studied ETN are obtained as shown in Fig. 14. They reveal acceptable temperature errors within 4.4%, 3.2%, and 2.0% for the Si die, die joint and baseplate joint, respectively, related to the T2. The errors can be because of the linear relationships assumed for the temperature of the layers with the affecting factors mentioned in the previous sections.
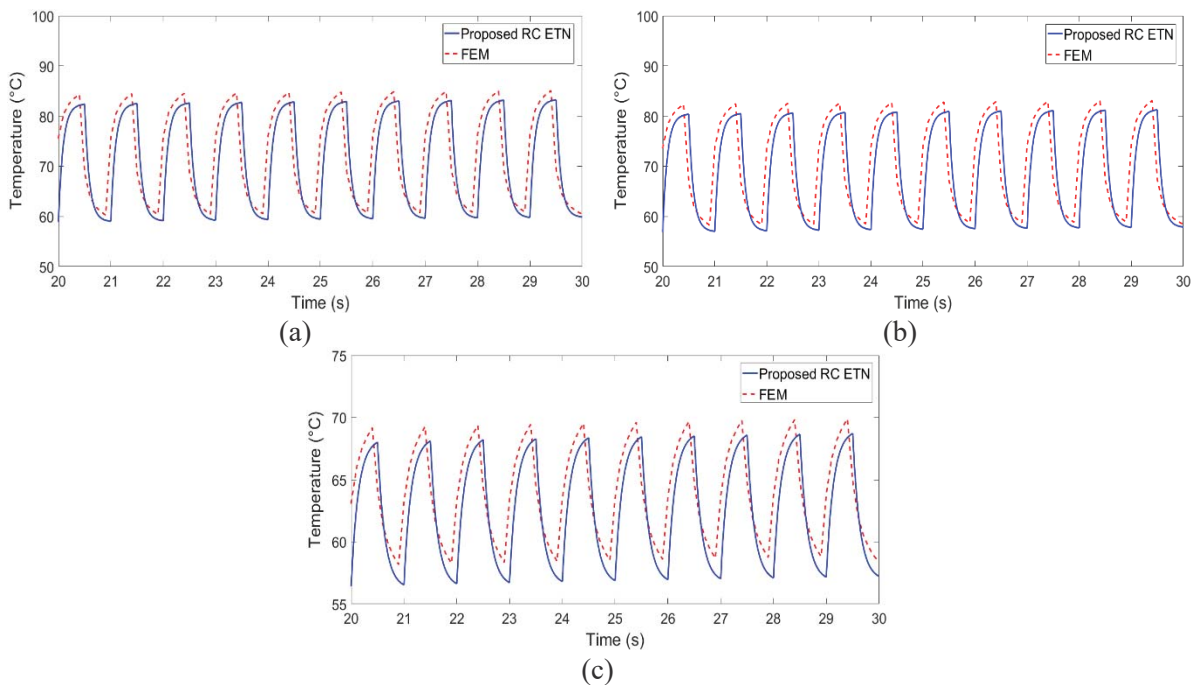

Fig. 14: Temperature curves obtained from the studied ETN and FEM for the T2:
(a) junction, (b) die joint, (c) baseplate joint

Conclusions

In this paper, a boundary condition-based Foster ETN for a multi-die Si IGBT module mounted on a heatsink is provided to simulate the temperature of different critical constituent layers, which also includes thermal coupling among dies. It is found that the ambient temperature and power loss affect the thermal RC model of both Si die and DBC substrate, while the cooling system mechanism influences the RC model of the heatsink, only. In addition, the ETN is developed to be adapted to the degraded IGBT module where circular voids, with an overall area of 50% and maximum 10% each, are devoted as conclusions of the thermal aging of Sn-Ag-based solder joints. It is figured out that the thermal resistance of solder joints significantly changes with the overall void area, while the heat capacitance is fixed. In this study, comparisons between the studied adaptive ETN and FEM verify the satisfactory performance of the ETN. While such an ETN has low computational time, it is robust in operation and over time and can provide valid temperatures for the lifetime prediction and thermal management of the power module with fair response times.

References

[1] Yang S., et al.: Condition monitoring for device reliability in power electronic converters: a review, IEEE Trans. Power Electron. Vol. 25 no. 11, pp. 2734-2752, Nov. 2010.

[2] Zhou M., Blaabjerg F., Lau M., and Tonnes M.: Thermal cycling overview of multi-megawatt two-level wind power converter at full grid code operation, IEEJ J. Ind. Appl. Vol. 2 no. 4, pp. 173-182, Jan. 2013.

[3] Saleki A., Changizian M., Rezazade S., and Bina M.T.: Lifetime extension by varying switching frequency of inverters based on junction temperature estimation, 9th Annu. Power Electron. Drives Syst. Technol. Conf. (PEDSTC), Tehran, Iran, pp. 259-264, Feb. 2018.

[4] Ma K., and Blaabjerg F.: Thermal optimized modulation methods of three-level neutral-point-clamped inverter for 10 MW wind turbines under low-voltage ride through, IET Power Electron. Vol. 5 no. 6, pp. 920-927, July 2012.

[5] Huanhuan W., Khambadkone A.M., and Xiaoxiao Y.: Control of parallel connected power converters for low voltage microgrid-Part II: dynamic electrothermal modeling, IEEE Trans. Power Electron. Vol. 25 no. 12, pp. 2971-2980, Dec. 2010.

[6] Ma K., Liserre M., and Blaabjerg F.: Reactive power influence on the thermal cycling of multi-MW wind power inverter, IEEE Trans. Ind. Appl. Vol. 49 no. 2, pp. 922-930, Mar.-Apr. 2013.

[7] Choi U.M., Blaabjerg F., Iannuzzo F., and Jørgensen S.: Junction temperature estimation method for a 600 V, 30A IGBT module during converter operation, Microelectron. Rel. Vol. 55 no. 9-10, pp. 2022-2026, Aug.-Sept. 2015.

[8] Avenas Y., and Dupont L: Evaluation of IGBT thermo-sensitive electrical parameters under different dissipation conditions-comparison with infrared measurements, Microelectron. Rel. Vol. 52 no. 11, pp. 2617-2626, Nov. 2012.

[9] Perpina X., et al.: Temperature measurement on series resistance and devices in power packs based on on-state voltage drop monitoring at high current, Microelectron. Rel., Vol. 46 no. 9-11, pp. 1834-1839, Sept.-Nov. 2006.

[10] Carubelli S., and Khatir Z.: Experimental validation of a thermal modelling method dedicated to multichip power modules in operating conditions, Microelectron. J. Vol. 34 no. 12, pp. 1143–1151, Dec. 2003.

[11] Bahman A.S., Ma K., Ghimire P., Iannuzzo F., and Blaabjerg F.: A 3D lumped thermal network model for long-term load profiles analysis in high power IGBT modules, IEEE Trans. Emerg. Sel. Topics Power Electron. Vol. 4 no. 3, pp. 1050-1063, Sept. 2016.

[12] Du B., et al.: Transient electrothermal simulation of power semiconductor devices, IEEE Trans. Power Electron. Vol. 25 no. 1, pp. 237-248, Jan. 2010.

[13] Filho G.C.K., et al.: A computational system for dynamic capacity analysis of distribution circuits-Finite volume method (FVM), IEEE PES Transm. Distrib. Conf. Expo. (T&D), Orlando, USA, pp. 1-6, May 2012.

[14] Bahman A.S., Ma K., and Blaabjerg F.: A lumped thermal model including thermal coupling and thermal boundary conditions for high power IGBT modules, IEEE Trans. Power Electron. Vol. 33 no. 3, pp. 2518-2530, Mar. 2018.

[15] Luo Z., Ahn H., and Nokali M.A.E.: A thermal model for insulated gate bipolar transistor module, IEEE Trans. Power Electron. Vol. 19 no. 4, pp. 902-907, July 2004.

[16] Roncati D.: Iterative calculation of the heat transfer coefficient, Progettazione Ottica Roncati, Italy, 2013.

[17] Alavi O., Viki A.H., Bina M.T., and Akbari M.: Reliability assessment of a stand-alone wind-hydrogen energy conversion system based on thermal analysis, Int. J. Hydrogen Energy Vol. 42 no. 22, pp. 14968-14979, June 2017.

[18] Morozumi A., Yamada K., Miyasaka T., Sumi S., and Seki Y.: Reliability of power cycling for IGBT power semiconductor modules, IEEE Trans. Ind. Appl. Vol. 39 no. 3, pp. 665-671, May-June 2003.

[19] Hunger T., and Bayerer R.: Extended reliability of substrate solder joints in power modules, 13th Eur. Conf. Power Electron. Appl. (EPE), Barcelona, Spain, pp. 1-8, Sept. 2009.

[20] Military Standard Test Methods and Procedures for Microelectronics, in MIL-STD-883D Method 2030, 1993, Department of Defense.

[21] Otiaba K.C., et al.: Numerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device, Microelectron. Rel. Vol. 52 no. 7, pp. 1409-1419, July 2012.